APPLICATION NOTE

ANP113 | Feedback loop compensation of a current-mode Flyback converter with optocoupler

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01. INTRODUCTION AND THEORETICAL BACKGROUND

The flyback converter is an isolated switching power supply topology widely used for output power levels below 150 W (Figure 1). In addition to providing galvanic isolation between input and output, it generates an output voltage which can be higher or lower than the input voltage. Its range of applications is vast, covering not only offline AC-DC conversion and power factor correction stages, but also high and low-voltage DC-DC converters alike in virtually all industry areas. A few example applications are main and auxiliary supplies for home-appliances, battery chargers for smartphones/tablets, LED lighting, computer/laptop power supplies, power-over-ethernet (PoE), industrial power, auxiliary supplies in motor drives, etc.

To keep the output voltage regulated at a target level despite variations in the input voltage or output current, the output voltage needs to be monitored and a related signal fed back to the controller, which can then adjust the duty-cycle of the control transistor regulating with it the flow of energy to the output. This is a closed-loop negative feedback system, with a plant block (formed by the duty-cycle generator and power stage), and with a compensator block, necessary to stabilize and shape the dynamic response of the converter (see Figure 2). Note that the compensator is designed to ensure not only that the feedback loop is stable, meaning that perturbation signals will not generate a sustained oscillation in the system, but also that after a transient event the output voltage will meet the target requirements regarding over- and undershoot, ringing and settling-time imposed by the supplied load.

In most isolated converters requiring tight output voltage regulation, an **optocoupler** is commonly used to transfer the feedback signal across the isolation barrier from the secondary side (compensator) to the primary side (controller). Optocouplers provide a mechanically-robust isolation barrier with very high voltage ratings (e.g. 5 kV) in a small package size, helping the power supply to meet stringent safety standards.

The optocoupler is then part of the control loop, and more exactly, of the compensator block. Therefore, parameters like its current-transfer-ratio (CTR) and collector-emitter parasitic capacitance appear in the compensator transfer function, modifying the amplitude and phase of the feedback signal. For this reason, their variations must also be considered in the design, otherwise the stability of the power supply could be compromised and the target transient response not met.

This application note provides an example procedure for designing the compensator circuit of a flyback converter with current-mode control and optocoupler-based feedback, including validation results in a prototype. Special attention is given to design limitations brought by optocoupler parameters and possible solutions are presented.
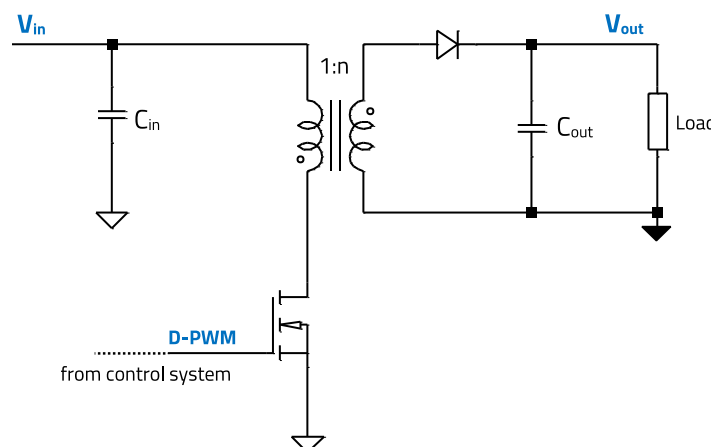

Figure 1: Flyback converter power stage (simplified)

02. BASICS OF FEEDBACK LOOP STABILITY OF SWITCHING POWER SUPPLIES

A flyback converter with its control loop is shown in Figure 2, with the transfer functions expressed in the Laplace s-domain. The plant of the system, with transfer function H(s) (a.k.a. control-to-output transfer function), is formed by the power stage (P(s)) and the duty-cycle generator block (G(s)). Note that the transfer function G(s) will vary depending on the control technique used, producing different plant characteristics for current-mode and voltage-mode control, for example, whereas the power stage transfer function P(s) is independent of the control technique. In Figure 2, a simplified duty-cycle generator block for a peak current-mode controller is shown, as it will be used in the design example of this document. Regarding the compensator, a Type 2 configuration with OP-AMP and optocoupler is illustrated. Such Type 2 compensator can be implemented with different circuits, the most common being OP-AMP (operational amplifier), TL431 (voltage reference with internal error amplifier, as in the design of this application note) and OTA (operational transconductance amplifier).
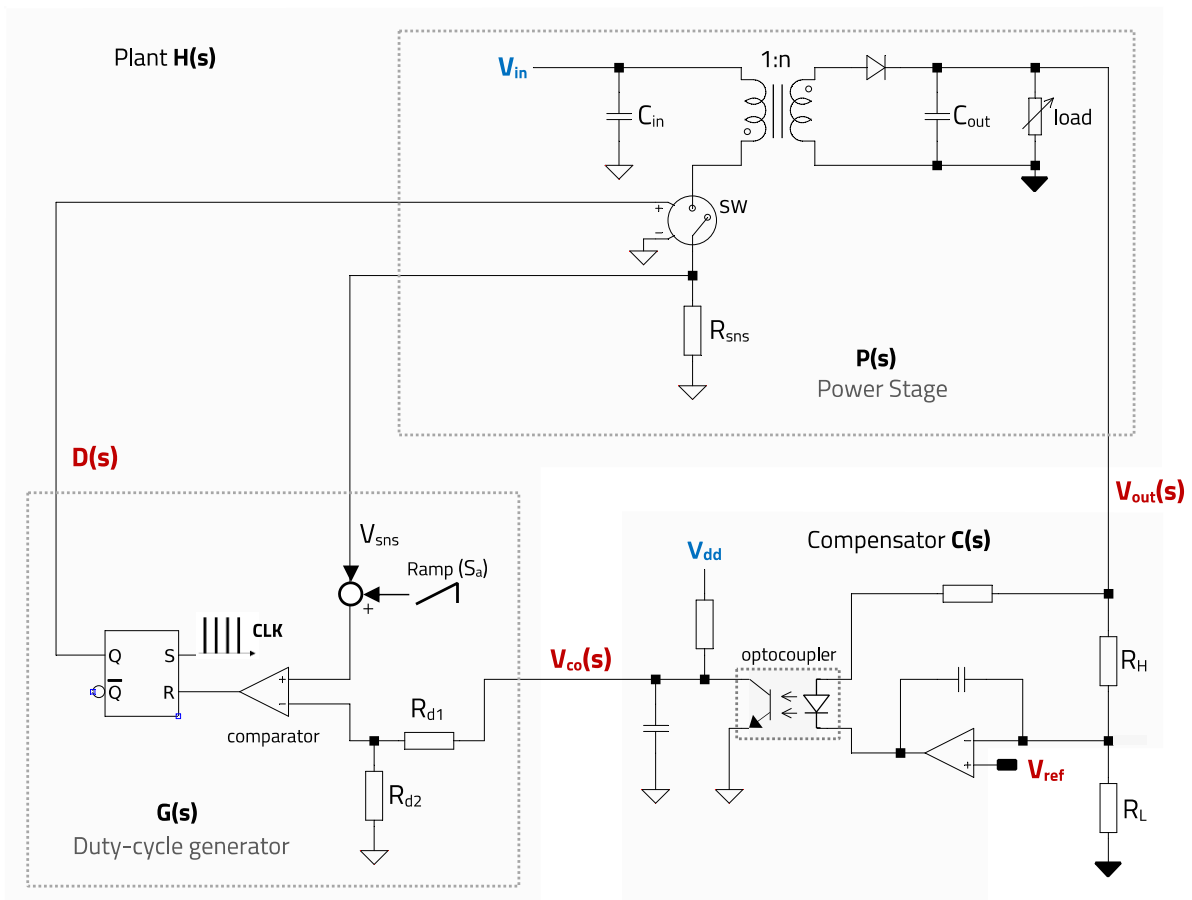

Figure 2: Example of Isolated peak current-mode control Flyback converter with optocoupler and OP-AMP compensator feedback (simplified).

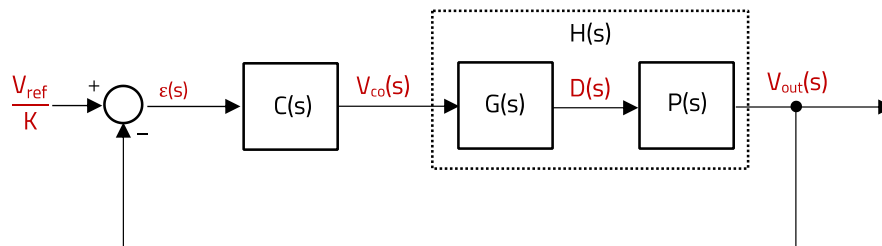The blocks in Figure 2 form the closed-loop feedback system of Figure 3:

Figure 3: Feedback Loop Block Diagram (unity-gain form)

Note in Figure 2 that the output voltage is reduced by a factor 'K' by the resistor divider formed by R_H and R_L, in order to scale it down for direct comparison to the reference voltage (V_{ref}) at the input of the error amplifier, with:

$$K = \frac{R_L}{R_H + R_L} \tag{1}$$

Applying transfer function block theory, the closed-loop transfer function for DC (s = 0) is:

$$G_{cl}(0) = \frac{v_{out}(0)}{v_{ref}} = \frac{1}{K} \cdot \frac{C(0) \cdot G(0) \cdot P(0)}{1 + C(0) \cdot G(0) \cdot P(0)} \tag{2}$$

The resistor divider factor 'K' only appears in the DC analysis. In a negative feedback system, the inverting input of the OP-AMP is held to the same DC voltage as the non-inverting input (V_{ref}) if a low-enough impedance exists between the output and the negative terminal of the device. In such case, the resistor R_L is effectively connected across two DC nodes, which are the same node for AC: an 'AC virtual ground'. The closed-loop transfer function for AC is:

$$G_{cl}(s) = \frac{C(s) \cdot G(s) \cdot P(s)}{1 + C(s) \cdot G(s) \cdot P(s)} \tag{3}$$

In the above, the product of transfer functions of the compensator and plant (i.e. the numerator) forms the open-loop transfer function $G_{ol}(s)$:

$$G_{ol}(s) = C(s) \cdot G(s) \cdot P(s) \tag{4}$$

From a strict theoretical definition, a stable closed-loop system is one which does not sustain oscillations. Based on the system of E.3, a condition for sustained oscillations is given by the Barkhausen criteria, as follows:

$$1 + C(s) \cdot G(s) \cdot P(s) = 0 \tag{5}$$

Expressed otherwise:

$$G_{ol}(s) = C(s) \cdot G(s) \cdot P(s) = -1 \tag{6}$$

This condition applied to the open-loop transfer function $G_{ol}(s)$ is translated to the following requirements for its modulus and phase:

$$|C(s) \cdot G(s) \cdot P(s)| = 1 = 0 \text{ dB} \tag{7}$$

$$\varphi_{Gol(s)} = -180° \tag{8}$$

Considering $s = j\omega = j2\pi f$, the frequency f_c at which E.7 condition is met is known as the crossover frequency ($|G_{ol}(f_c)| = 0$ dB). Since Laplace s-domain analysis refers to sinusoidal signals, considering a sinusoidal perturbation in the system, the conditions in E.7 and E.8 mean that if the phase shift provided by the open-loop transfer function at the crossover frequency is -180°, then the system will sustain oscillation at f_c, and will therefore be unstable.
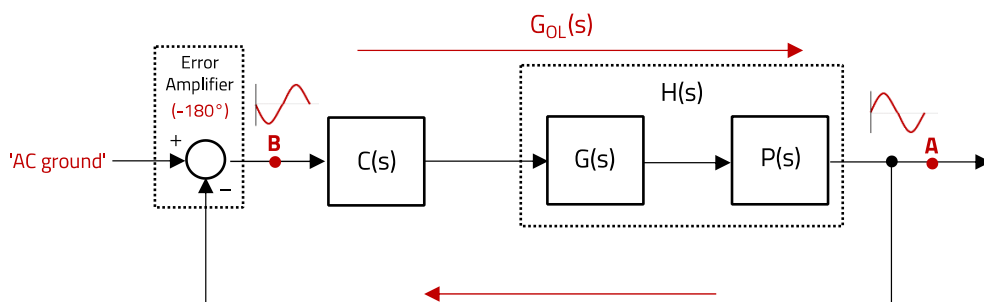

Figure 4: Example sinusoidal perturbation propagating around the feedback loop

Figure 4 shows intuitively this concept. A sinusoidal perturbation arising at point 'a' in the loop, will become phase shifted -180° by the negative feedback (i.e. inverting action) of the error amplifier. If it suffers a further -180° phase shift as it passes through the compensator and plant, which form the open-loop transfer function, it will return exactly in phase at the origin point. If the gain provided by the open-loop transfer function is exactly '1', the perturbation will return with the same amplitude, generating a sustained oscillation.

Phase margin (PM)

The phase margin is an indication of how much phase shift a sinusoidal signal of frequency equal to f_c would need to undergo to make the system unstable. Based on the diagram of figure 4, it corresponds to the difference between the phase of the open-loop transfer function at the crossover frequency (0 dB) and -180°:

$$PM = \varphi_{G_{ol}(fc)} + 180° \tag{9}$$

Note that the conditions previously shown on E.7 and E.8 only refer to sustained oscillations. However, if the phase margin is too low, although the system is considered 'stable' from a theoretical point of view, the output voltage response to a transient event will present oscillations whose amplitude will decay with time (a.k.a. ringing). This may not be acceptable to many systems having to meet stringent specifications regarding overshoot, undershoot and settling time. Figure 5 shows an example transient response of a closed-loop system with a fixed crossover frequency (3 kHz) but different phase margins: PM = 30°, 45°, 60° and 75°. It is observed how, as the phase margin increases, the system response presents less ringing. How much phase margin to select depends on the target transient response, but a worst-case phase margin higher than 45° should be ensured. Note also that a faster settling time can also be achieved by increasing the open-loop crossover frequency.
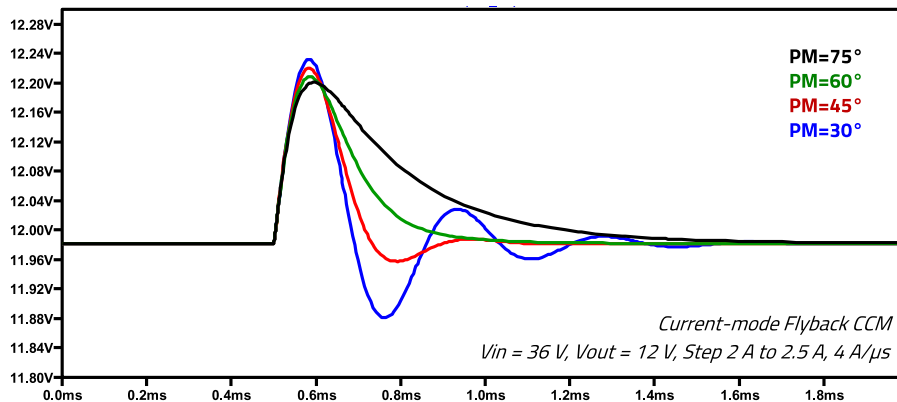

Figure 5: Example transient response for f_c = 3 kHz and various phase margin values (LTspice™ simulation)

Gain Margin (GM)

The gain margin indicates how much gain the system can tolerate before becoming unstable, and it is relevant when considering tolerances of component values or the effect of an underdamped double pole in current-mode control systems. Based again on figure 4, it corresponds to the magnitude of the open-loop transfer function at the frequency where its phase reaches -180° (f_{gm}).

$$GM = \left| G_{ol}\left(f_{gm}\right) \right| \tag{10}$$

Note that a gain margin higher than 10 dB should be targeted as a general rule-of-thumb [3].

Compensator Specification

Since the transfer function of the power stage and duty-cycle generator are mostly fixed by the converter design specification and control technique used, a 'compensator' circuit is necessary to set the target open-loop crossover frequency and phase margin.

The compensator block will need to provide the gain or attenuation required to make the open-loop transfer function to cross over at the target f_c, and will also need to provide the required phase boost at the crossover frequency in order to meet the phase margin specification, while ensuring enough gain margin. Expressing this mathematically:

$$C_{dB}(f_c) = -H_{dB}(f_c) \qquad (11)$$

$$\varphi_{comp\_boost}(f_c) = PM - 90 - \varphi_{plant}(f_c) \qquad (12)$$

It is important to note that in the LTspice™ and MATLAB™ plots shown in this document, the phase range used is between -180° and +180°. In this format, +360° would be added to any phase values between -180° and -360° (e.g. a phase of -250° will appear represented as +110°). In addition to this, the inverting action of the error amplifier (-180°) is already included in the plotted compensator phase curve, since the compensator circuit is built around the error amplifier. Taking into account this format, the phase margin will be directly read as the open-loop phase at f_c, and the gain margin as the open-loop gain at the frequency where its phase crosses 0°. In order to understand equation 12, the permanent phase provided by the compensator must be observed. This is formed by the origin pole used to minimize the DC error of the system (integrator action), providing a constant phase of -90°, plus the -180° of the inverting action of the error amplifier. The compensator permanent phase lead is then -270° (i.e. +90°). To this value, the compensator phase boost φ_{comp_boost} is added to form the total compensator phase.

Figure 6 shows the transfer function plots of the plant ($V_{(out)}$, red, cursor 1), compensator ($V_{(ol)}/V_{(out)}$, green, cursor 2/cursor 1) and the resulting open-loop response ($V_{(ol)}$, black, cursor 2)) of an example design like the one presented in this document, as simulated in LTspice™. Note that solid lines correspond to the magnitude (dB) (left axis), whereas dotted lines to the phase (deg) (right axis) of the corresponding transfer function. In this example, the plant shows a gain of -1.41 dB at f_c = 2.88 kHz and -80.7° phase. The compensator provides a gain of +1.41 dB and a phase boost of around 60° at 'f_c' (151.5° - 90°). As a result, the open loop transfer function crosses 0 dB at 2.88 kHz with a phase margin of 151.5° - 80.7≈70°, and the gain margin is around 20 dB. This is an example of a stable feedback loop design.
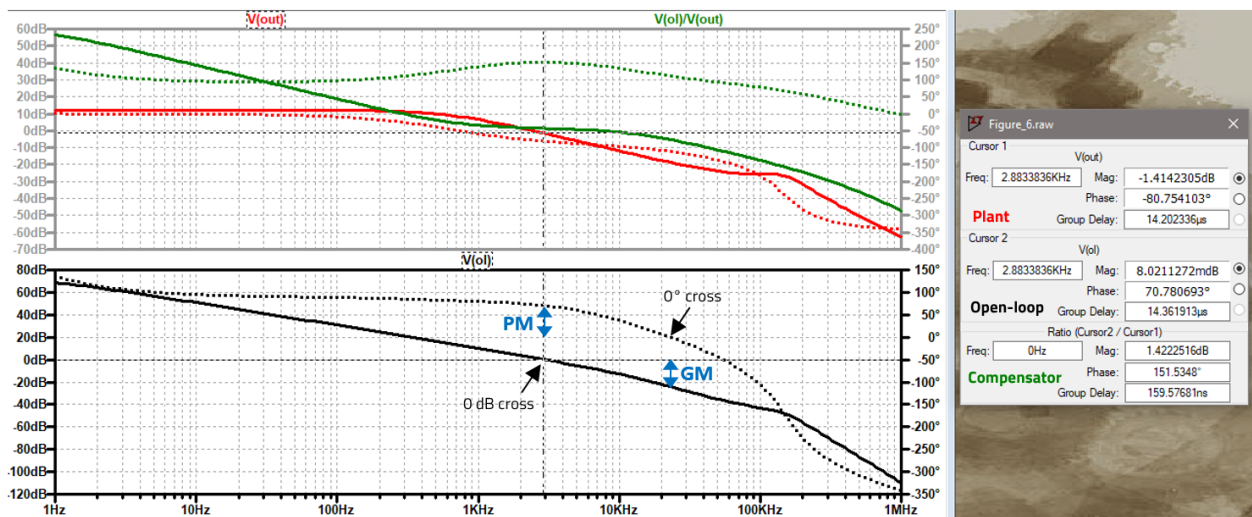

Figure 6: Example of plant, compensator and open-loop transfer function Bode plots showing (f_c), PM and GM (LTspice™ Simulation)

03. THE PLANT (CONTROL-TO-OUTPUT) TRANSFER FUNCTION OF A CURRENT-MODE FLYBACK CONVERTER

Once the design of the converter power stage is completed, the first step in the compensation procedure is to study the characteristics of the plant transfer function formed by the power stage and the duty-cycle generator. Note that the plant transfer function will be different depending on whether the converter operates in continuous conduction mode (CCM) or in discontinuous conduction mode (DCM), so both conditions need to be considered.

For the analysis, the design specifications used are the following, based on the design prototype presented later in section 010:

$$V_{in} = 36 - 57 \text{ V}, \ V_{out} = 12 \text{ V}, \ I_{out_{max}} = 2.5 \text{ A}, \ F_{sw} = 300 \text{ kHz}, \ L_m = 41 \text{ µH}, \ C_{out} = 100 \text{ µH}, \ ESR_{Cout} = 280 \text{ µ}\Omega$$

For the above specification, the converter will enter DCM operation for an output current of around 1.25 A.

The transformer used in the design is the WE-PoEH 7491195112 [8] from Würth Elektronik and the IC controller the NCP12700 from onsemi [9]. This IC integrates the simplified duty-cycle generator block shown in previous figure 2, in addition to many other relevant safety and functional features. It is observed that the compensator output voltage V_{co} is divided by resistors R_{d1} and R_{d2}, before being fed to the peak current setting comparator (fig. 2). In the case of the NCP12700, the divider factor is $V_{div}=6$ (i.e. $R_{d1}=5 \cdot R_{d2}$). This means that the magnitude of the plant transfer function is also divided by '6' in this case, as the resistor divider is like a simple gain block in the feedback path. Since at the highest power demand (highest magnetizing peak current) $V_{(co\_max)} \approx V_{dd}$, which is typically around 5 V (see [9]), , the resistor divider will produce in this case a voltage $V_{(co\_div)} = 833$ mV at the comparator input. Such low voltage allows to select a lower value of the current sense resistor for the same peak current setting, improving with it efficiency, while still allowing the compensator output voltage to keep a wide dynamic range (0.2 to 5 V).

Regarding the added compensation ramp (S_a), it is generated internally by the NCP12700 and it is variable, meaning that its slope is adjusted depending on the switching frequency and duty-cycle. A table of values is provided as a reference in the datasheet. For $F_{sw} \approx 300$ kHz as in this design, the generated compensation slope is found in the range between 33 kV/s and 81 kV/s.

3.1 Continuous Conduction Mode Operation (CCM)

The plant transfer function of a current-mode flyback converter operating in CCM is of the form [1]:

$$H(s) = \frac{V_{out}(s)}{V_{co}(s)} = G_o \cdot \frac{\left(1 + \frac{s}{\omega_z}\right) \cdot \left(1 - \frac{s}{\omega_{rhpz}}\right)}{\left(1 + \frac{s}{\omega_p}\right) \cdot \left(1 + \frac{s}{Q_p \cdot \omega_n} + \frac{s^2}{\omega_n^2}\right)} \tag{13}$$

It features a DC-gain (G_o), a zero (ω_z), a right-half plane zero (ω_{rhpz}), a pole (ω_p) and a double-pole at half of the switching frequency (ω_n), which models the subharmonic oscillation instability as the duty-cycle approaches and exceeds 50% in a peak current-mode converter.

Prior to selecting a crossover frequency and to design the compensator, it is necessary to plot the magnitude and phase versus frequency of the plant transfer function (i.e. Bode plot). This can be done in different ways: from an analytical small-signal model of the converter [1], via a SPICE simulation with an averaged PWM switch model [2], or measuring it directly if a prototype is available.

Figure 7 shows the plant transfer function characteristic for the design specification above, albeit without slope compensation ramp applied ($S_a = 0$). The results are based on the analytical model provided in [1], and plotted using MATLAB™. Considering E.13, the following values are obtained for minimum input voltage (36 V) and full load (2.5 A):

$$G_o = 13.1 \text{ dB}, \ f_z = 5.05 \text{ MHz}, \ f_p = 530 \text{ Hz}, \ f_{rhpz} = 74.4 \text{ kHz}, \ f_n = 150 \text{ kHz}, \ Q_p = 17.1$$
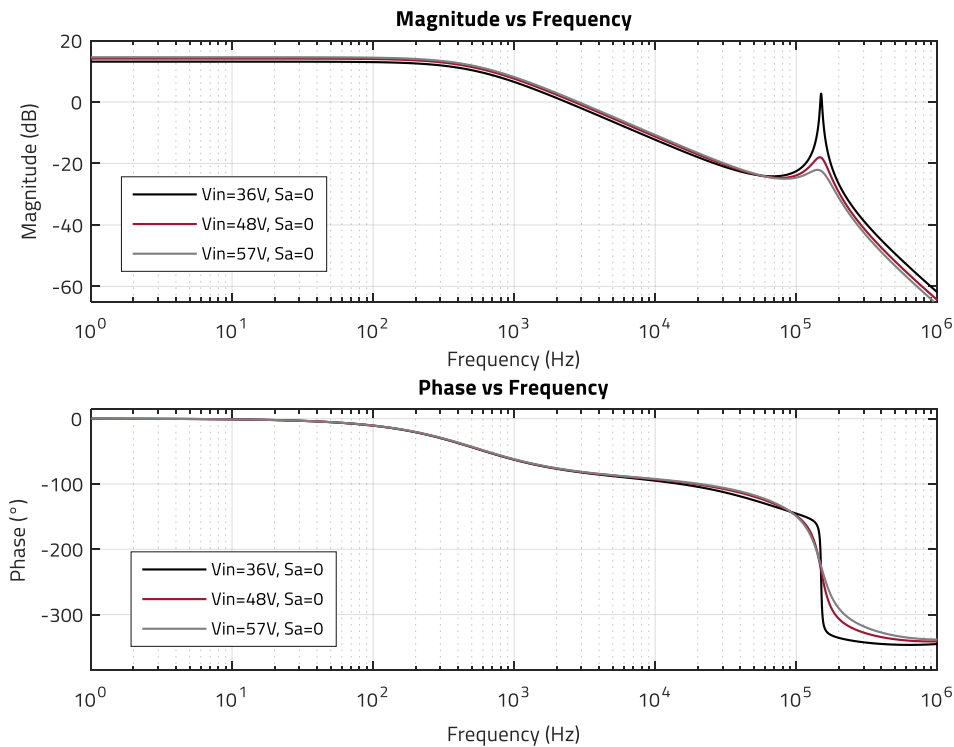
Figure 7: Plant transfer function in CCM operation for Vin range (36 V, 48 V, 57 V) and $S_a = 0$ (MATLAB™)

The magnitude curve presents a 1st order characteristic in the lower frequency range. Note that the zero formed by the output capacitor and its ESR (ω_z) happens at a very high frequency, and it is therefore out of the range of interest. This is due to the extremely low ESR value (out of paralleling 12 x MLCC WCAP-CSGP-**885012109010**). This means that special considerations regarding ESR variations are not necessary, but any beneficial phase boost provided by this zero in the lower frequency range is lost. Although in this design the right-half-plane zero also happens at a relatively high frequency, it starts to contribute phase lag at around one decade before, and it is typically the main constraint in selecting the crossover frequency.

It is observed how the double-pole causes a dramatic phase drop at $f_n = f_{sw}/2$. At minimum input voltage (D = 49%) and without compensation ramp the quality factor (Q_p) is very high, 17.1, signaling instability with the high peaking of the plant transfer function magnitude at f_n. For nominal and maximum input voltages, the duty-cycle is 42% and 38%, respectively, with a quality factor of 3.56 and 2.44, and a much lower peaking is observed. Excessive peaking degrades the gain margin and can make the system unstable when causing the magnitude of the open-loop transfer function to cross over 0 dB more than once, complicating stability analysis.

Some compensation ramp is therefore necessary to 'damp' the peaking. The minimum value of compensation ramp required to ensure stability at all duty-cycles is:

$$S_a \geq 0{,}5 \cdot S_2 \tag{14}$$

where S_2 is the magnetizing current slope during the off-time of the power inductor/transformer, as sensed through the sensed resistor R_s, with units of kV/s:

$$S_2 = \frac{V_{out} + V_f}{n \cdot L_m} \cdot R_s \tag{15}$$

The transformer turns-ratio 'n' is 0.374 and the above expression yields $S_a \geq 61$ kV/s. It should be noted, however, that the converter does not need ramp compensation for all duty-cycles. Since $D_{max} = 0.49$, a lower slope compensation will suffice. This is confirmed by plotting the plant transfer function for $S_a = 30$ kV/s and $S_a = 80$ kV/s, as shown in Figure 8 and Figure 9. The peaking is well damped even at the minimum expected compensation ramp.
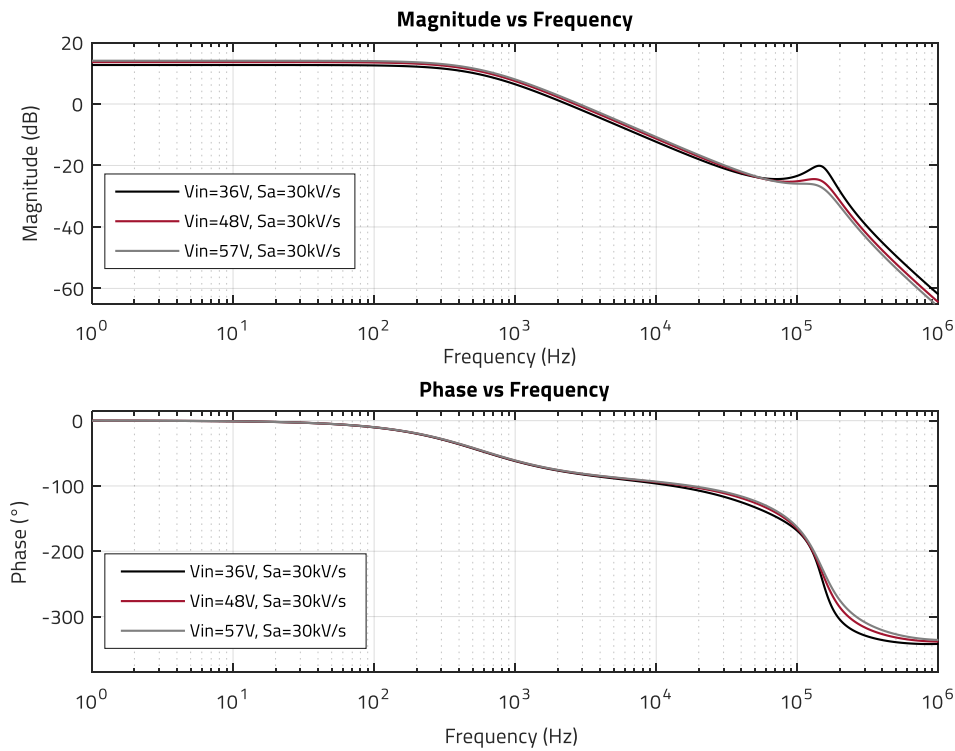
Figure 8: Plant transfer function in CCM operation for V_{in} range (36 V, 48 V, 57 V) and S_a = 30 kV/s (MATLAB™)

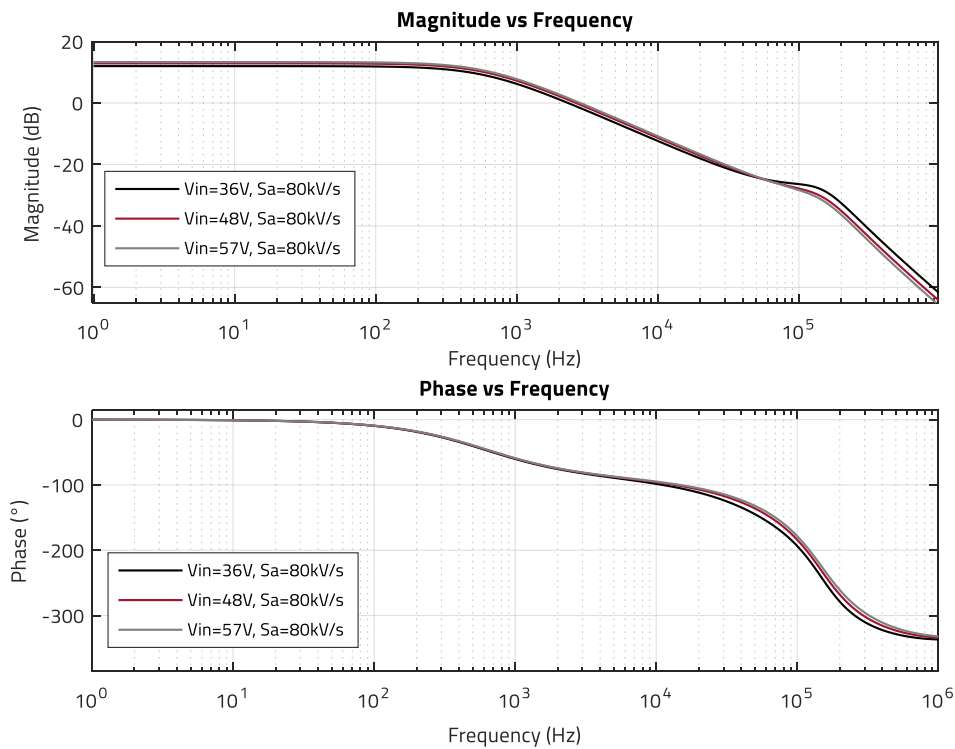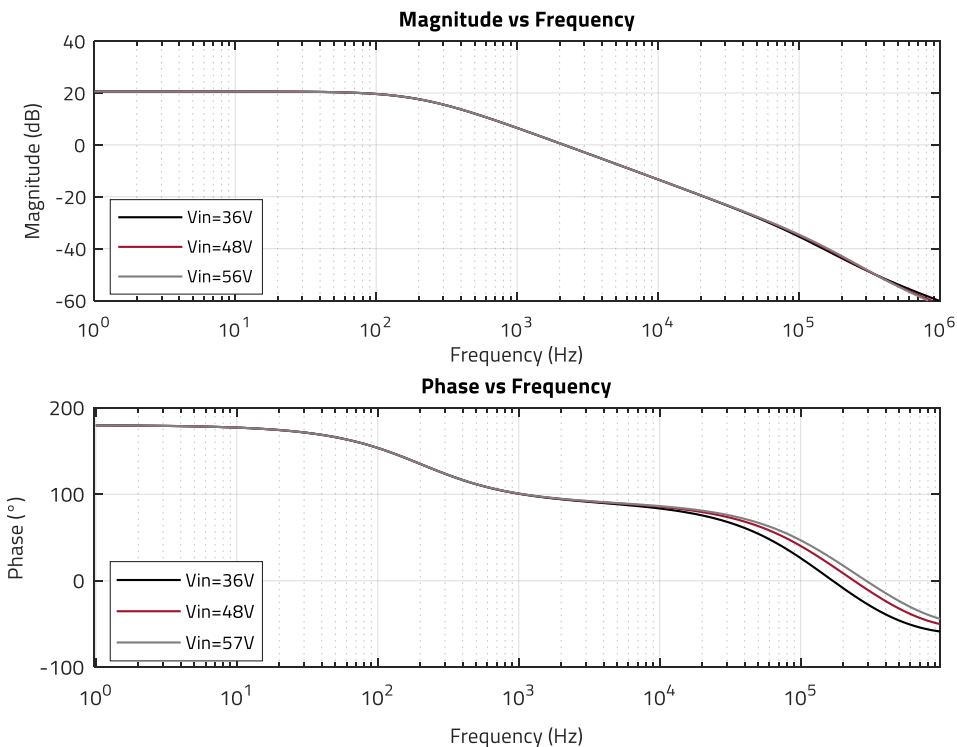Figure 9: Plant transfer function in CCM operation for V_{in} range (36 V, 48 V, 57 V) and S_a = 80 kV/s (MATLAB™)

3.2 Discontinuous Conduction Mode Operation (DCM)

The control-to-output transfer function of a current-mode flyback converter operating in DCM is of the form [1]:

$$H(s) = \frac{V_{out}(s)}{V_{err}(s)} = G_o \cdot \frac{\left(1 + \frac{s}{\omega_z}\right) \cdot \left(1 - \frac{s}{\omega_{rhpz}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)} \tag{16}$$

As observed, in DCM there is no subharmonic oscillation instability and therefore no double-pole in the model. There is a right-half-plane zero but it happens at a higher frequency than in CCM. The same applies to the additional second pole and the ESR zero. For this reason, in the low-frequency range the current-mode flyback converter in DCM can be approximated by a single pole system, dominated by ω_{p1}, where:

$$\omega_{p1} = \frac{2 \cdot I_{out}}{V_{out} \cdot C_{out}} \tag{17}$$

As the output current reduces, the pole moves to a lower frequency. The values in this case, for V_{in} = 36 V, I_{out} = 0.8 A and S_a = 0 are:

$$G_o = 20.6 \text{ dB}, \ f_z = 5.05 \text{ MHz}, \ f_{p1} = 202 \text{ Hz}, \ f_{rhpz} = 247 \text{ kHz}, \ f_{p2} = 107 \text{ kHz}$$

Figure 10 shows the Bode plot of the DCM plant transfer function for input voltages of 36 V, 48 V and 57 V, and 0.8 A output current:

Figure 10: Plant transfer function in DCM operation for V_{in} range (36 V, 48 V, 57 V) and S_a = 0 kV/s (MATLAB™)

In previous Figure 7 to Figure 10 a common feature of current-mode control is clearly observed: the frequency response does not depend (almost) on the input voltage. Any input voltage variation will directly affect the slope of the magnetizing current. For a specific current peak setpoint, this will in turn change the duty cycle allowing for more or less energy transfer to the secondary side to keep the output power constant, without the need of causing an overshoot or drop of the output voltage to make the control loop react. This inherent feed-forward functionality is one of the main advantages of the current-mode control technique.

04. COMPENSATOR REQUIREMENTS

As seen in previous section, CCM operation presents higher requirements for compensation than DCM. Therefore, the compensator is typically designed for CCM at worst-case operating conditions (i.e. minimum input voltage and full load current), checking also the behavior for DCM to ensure it is still acceptable, and performing any necessary adjustments to obtain the required performance in both cases.

The target crossover frequency of the open-loop transfer function is selected to be anywhere below 1/5th of the switching frequency (for switching frequency noise attenuation), or 1/5th of the minimum right-half-plane zero frequency, whichever is lower. In many cases, the right-half-plane zero becomes the limiting factor, as in this design example. Note that the above is simply a rule-of-thumb for a very stable design, but different margins can also be used at the discretion and preference of every designer. In this case:

$$F_{c1} = \frac{F_{sw}}{5} = 60 \text{ kHz} \tag{18}$$

$$f_{rhpz\_min} = \frac{(1-D_{max})^2 \cdot R_{Lmin}}{2 \cdot \pi \cdot D_{max} \cdot n^2 \cdot L_{p\_max}} = \frac{(1 - 0{,}49)^2 \cdot 4.8}{6.28 \cdot 0.49 \cdot 0.374^2 \cdot 41 \text{ μ}} = 70.7 \text{ kHz} \tag{19}$$

$$F_{c2} = \frac{F_{rhpz\_min}}{5} = 14.4 \text{ kHz} \tag{20}$$

The crossover frequency should then be set lower than 14 kHz. The frequency area of interest for compensation is highlighted in Figure 11:
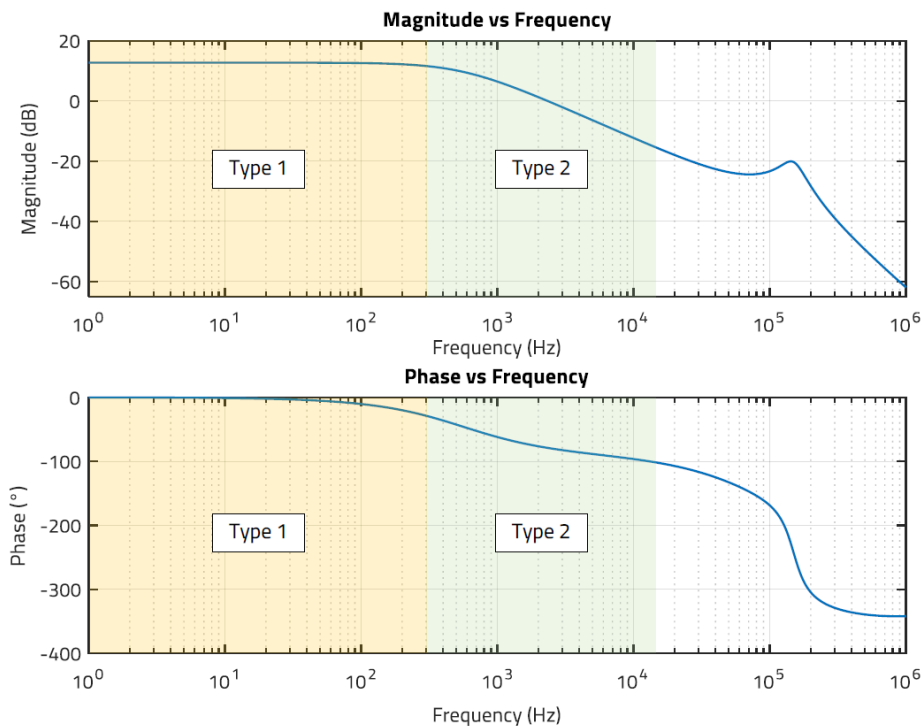
Figure 11: Frequency range of interest for crossover frequency selection and suitable compensator type

In the frequency range of interest (below 14 kHz), the plant shows a 1st order characteristic after the dominant pole of the system even in CCM operation (green) (slope of -20 dB/dec). In this area a Type 2 compensator is typically used, as it can provide the required gain and a phase boost up to 90°. If the crossover frequency is selected below the dominant pole (yellow), a simple Type 1 compensator (integrator-only) can be used to just provide high DC gain to minimize the static DC-error without any phase boost. It is observed that at such low frequency range the plant's phase shift is nearly zero, reaching -45° at the frequency of the dominant pole, and a phase margin from 45° to 90° can then be achieved with a simple Type 1 compensator.

It must be noted however that a lower crossover frequency has the drawback of a lower closed-loop bandwidth, which in turn causes a slower reaction of the closed loop system to changes in the output voltage, leading to higher overshoot, undershoot and settling time. Therefore, a compromise between transient performance and high-frequency noise attenuation needs to be found when selecting the crossover frequency. Note that adding more output capacitance can also help to improve the transient characteristic despite a low crossover frequency, albeit with the added cost.

In this case, a target crossover frequency of f_c = 10 kHz is (initially) selected, with a target phase margin of PM = 70°. The magnitude and phase of the control-to-output transfer function at f_c are shown in Figure 12:
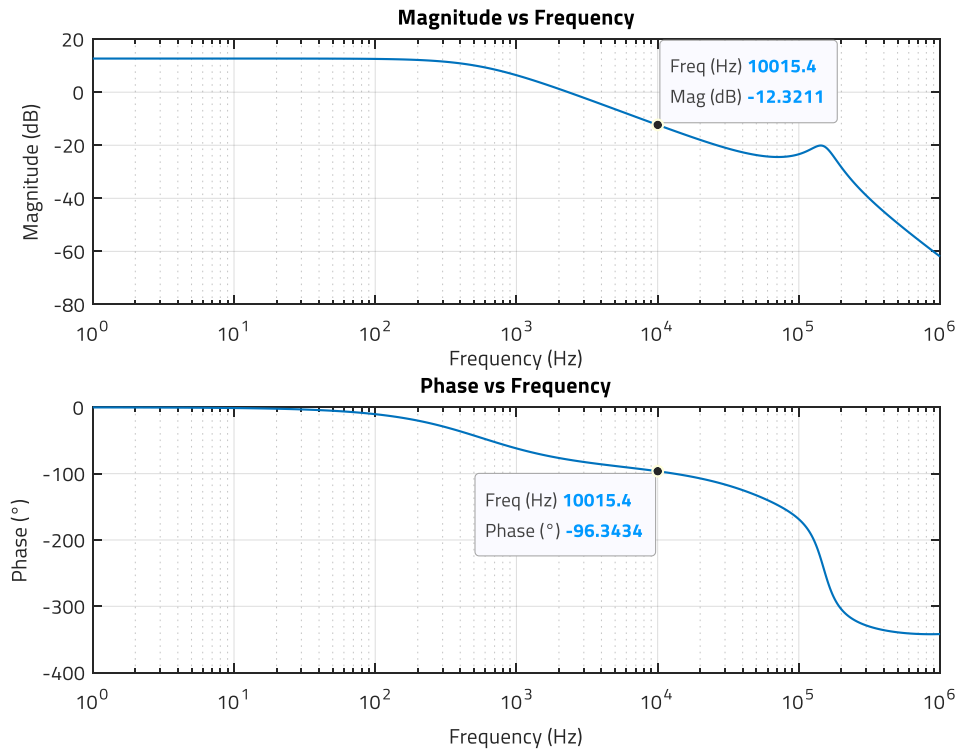
Figure 12: Magnitude (dB) and Phase (deg) of plant transfer function at f_c = 10 kHz (MATLAB™)

With a Type 2 compensator, the maximum phase margin achievable in this case is 83.6°, which is enough for the 70° target.

The compensator needs to provide a gain of +12.3 dB (equivalent to 4.12 unitless), to offset the plant gain and make the magnitude of the open-loop transfer function to cross over at f_c =10 kHz:

$$C_{dB}(f_c) = -H_{dB}(f_c) = 12.3 \text{ dB}$$

$$|C(f_c)| = 4.12$$

With a target phase margin of 70°, the phase boost that the compensator needs to provide at f_c is:

$$\varphi_{comp\_boost}(f_c) = PM - 90 - \varphi_{plant}(f_c) = 76.4°$$

05. DESIGN OF A TYPE 2 COMPENSATOR WITH TL431 AND WL-OCPT OPTOCOUPLER

With the compensator requirements set, a Type 2 compensator circuit needs to be selected. A very popular configuration for an isolated current-mode Flyback converter is based on the TL431 voltage reference and an optocoupler as shown in figure 13. This solution is widely used due to its low-cost, simple design and good enough performance.
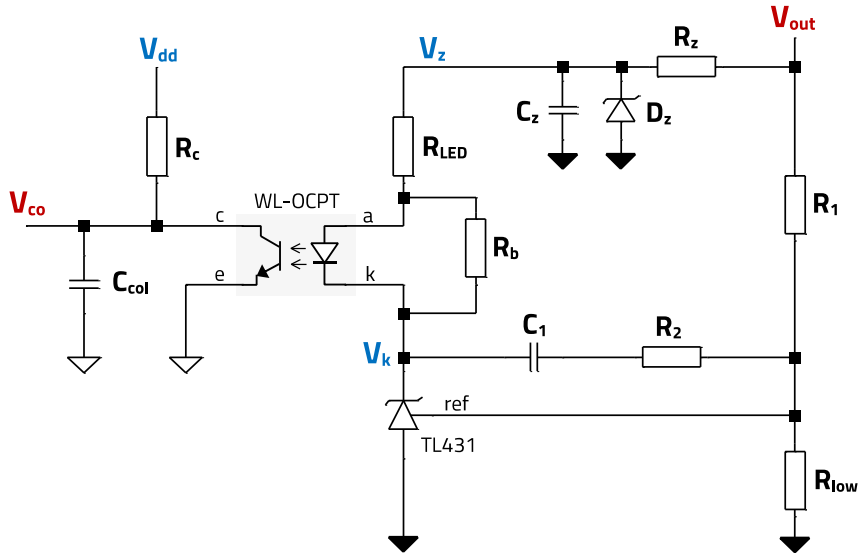

Figure 13: Type-2 compensator circuit with TL431 and WL-OCPT optocoupler

5.1 Circuit Operation

In Figure 13, it is observed that the optocoupler is biased in a common-emitter configuration, and so as the current through the LED increases, the collector-emitter voltage (V_{co}) decreases. Note that, based on previous Figure 2, V_{co} sets the magnetizing peak current and this way, indirectly, also the amount of energy transferred to the output. The TL431 sets the current through the LED by adjusting its cathode voltage (V_k), based on the output voltage (V_{out}). The TL431 acts like an error amplifier, and its internal structure is shown in figure 14 (based on the datasheet [10]).
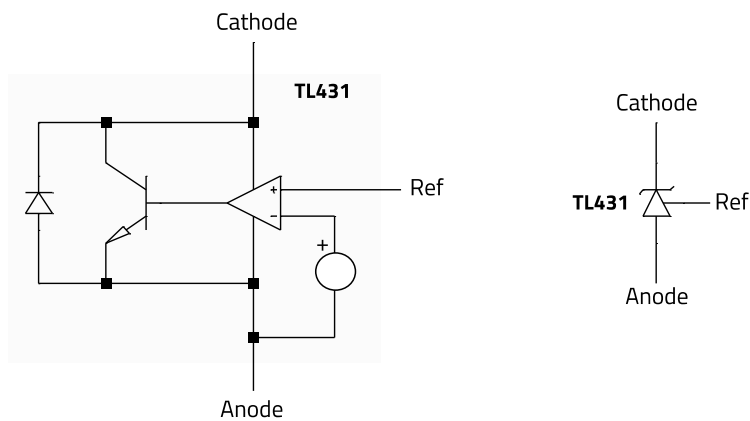
Figure 14: TL431 internal circuit [10]

When the voltage in the 'Ref' terminal is higher than the internal fixed reference voltage of the TL431, caused for example by an output voltage overshoot due to a sudden reduction in the load current, then more current is fed into the base of the npn transistor, and the cathode voltage of the TL431 decreases (change in operating point of the npn transistor within active region). This causes a higher voltage across R_{LED} and the optocoupler LED, with the subsequent increase in the LED current and, in turn, in the collector current. A higher collector current causes a higher voltage drop across R_c, resulting in a lower collector-emitter voltage, which in this configuration, represents the compensator output voltage (V_{co}). A lower V_{co} sets a lower peak

current setpoint, reducing the magnetizing current amplitude and, with it, reducing the amount of energy transferred to the secondary side. The output voltage is then brought back to the target regulated level. The opposite happens when there is a sudden increase in load current. Figure 15 illustrates this principle of operation for both, high-to-low and low-to-high load current steps (2.5 A to 2 A), for the specifications of this design.

Note:

V(co_{div}):	$V_{co}/6$ (the voltage at the comparator input after dividing the compensator voltage by V_{div} = 6)
V(cs_{leb}):	This is the voltage across the sense resistor R_s to which the compensation ramp is added (Sa = 55 kV/s)
I(Lp):	Transformer Primary winding current (magnetizing current)
V(tl431_k):	Voltage at the cathode of the TL431
Ix(U1:A):	LED current
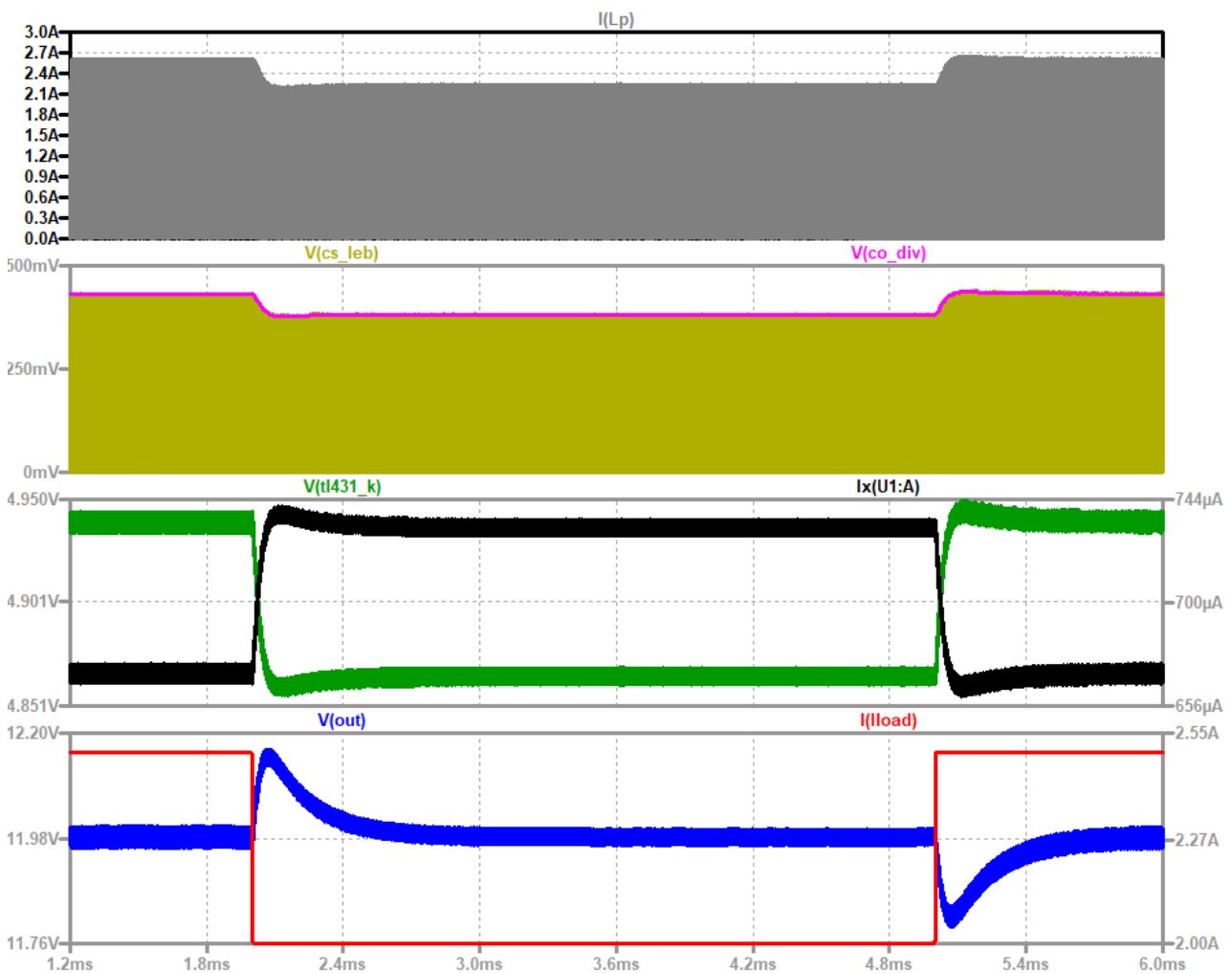
Figure 15: Example transient waveforms of the Type 2 compensator with TL431 and WL-OCPT optocoupler (LTspice™)

5.2 DC-Biasing the TL431 and WL-OCPT Optocoupler

For the compensator circuit to operate as described, the TL431 and optocoupler need to be DC-biased correctly. Specifically, the internal npn transistor of the TL431 and the output phototransistor of the optocoupler need to be biased in their active region for dynamic performance, and stay so even after any expected variations and tolerances of parameters are factored in.

For the optocoupler circuit, R_c = 5 kΩ and V_{dd} = 5 V are internally set in the NCP12700 controller [9].

Regarding the TL431 device [10], it requires a minimum cathode bias current of 1 mA and the minimum cathode voltage equals the reference voltage, in this case, 2.5 V.

The LED of the WL-OCPT 817 series has a worst-case minimum forward voltage drop of 0.85 V at 0.1 mA and 110°C (Figure 16). Adding a resistor (R_b) in parallel with the LED is a common technique used to generate a mostly constant current source for the TL431, since in normal operation there is always current flowing through the LED, and the voltage applied across R_b will be the forward voltage drop of the LED (V_f). Considering a minimum TL431 bias current of $I_{b\_TL431\_min}=2$ mA, the maximum allowable resistor value is:

$$R_{b\_max} = \frac{V_{f\_min}}{I_{b\_TL431}} = \frac{0.85\text{ V}}{2\text{ mA}} = 425\ \Omega \tag{21}$$
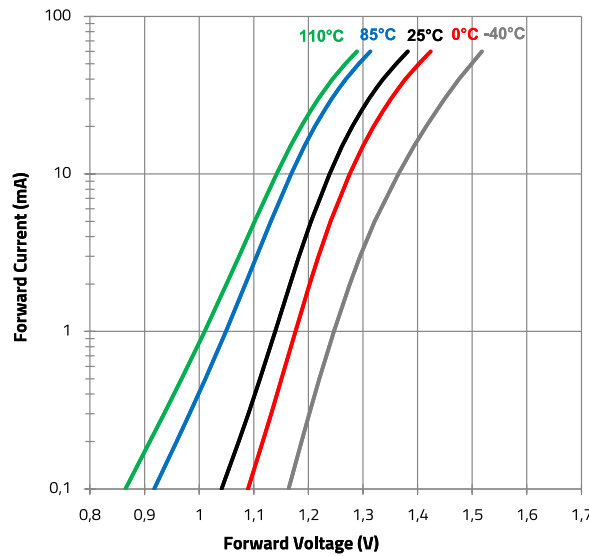
Figure 16: WL-OCPT 817 series - LED forward voltage vs forward current curve as a function of ambient temperature

Regarding the minimum TL431 bias voltage (V_{k_min}), we have:

$$V_k = V_z - V_{R_{LED}} - V_f \tag{22}$$

The maximum voltage drop across the LED resistor ($V_{R\_LED\_max}$) happens at the maximum LED current (I_{LED_max}), which in turn happens when the collector voltage is lowest ($V_{ce\_min} = V_{ce\_sat} = 0.2$ V). This in turn implies maximum collector current at the minimum absolute CTR, as follows:

$$I_{LED\_max} = \frac{I_{c\_max}}{CTR_{min}} = \frac{V_{dd}}{R_c \cdot CTR_{min}} \tag{23}$$

The value of the LED resistor needs to be lower than:

$$R_{LED\_max} \leq \frac{(V_z - V_f - V_{ref}) \cdot CTR_{min} \cdot R_c}{\left(V_{dd} - V_{ce\_sat} + I_{b\_TL431} \cdot CTR_{min} \cdot R_c\right)} \tag{24}$$

To calculate R_{LED_max}, it is necessary first to estimate the minimum CTR value of the WL-OCPT optocoupler. An example procedure for this is presented next.

Estimating minimum CTR of WL-OCPT optocoupler

The optocoupler CTR is affected by wide variations caused not only by technology and manufacturing tolerances but also by its dependence upon parameters like LED current, ambient temperature and operating time.

In order to reduce the CTR range to consider for a specific design, the WL-OCPT optocoupler series are classified in 'binnings', each of which guarantees a CTR value within a certain range for a specific DC-Bias condition, as the table in Figure 17 shows.

Test Condition	Binning	Min.	Max.	Unit
I_F = 5 mA V_{CE} = 5 V	None	50	600	%
	A	80	160	%
	B	130	260	%
	C	200	400	%
	D	300	600	%

Figure 17: Example of WL-OCPT optocoupler CTR binning for **817** and **816** series

Choosing a device from the 'A' binning means the CTR will range from 0.8 to 1.6 out of the production line. However, this is valid only for an LED current of 5 mA and a collector-emitter voltage of 5 V. For different specifications, the CTR range needs to be recalculated. The absolute CTR curve provided in the WL-OCPT datasheet for all binnings shows this dependence (Figure 18).
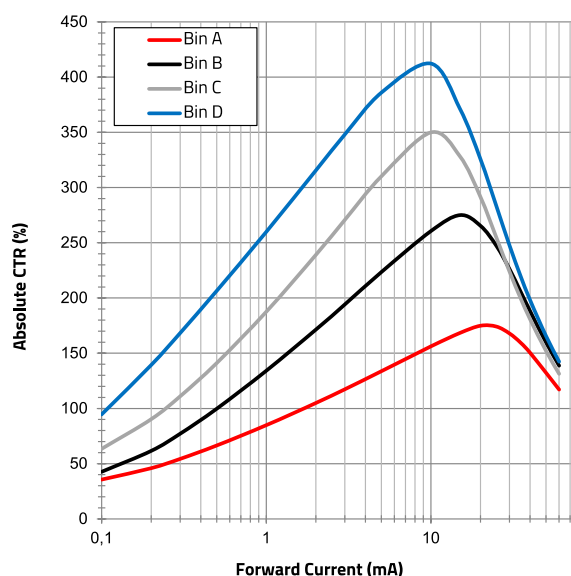
Figure 18: **WL-OCPT 817** Series: Absolute CTR vs. LED forward current (at V_{ce} = 5 V)

For more detailed information on the basics of optocouplers, please see **Application Note** on reference [12].

The DC bias conditions of the optocoupler at the operating point of interest must be known in order to estimate the minimum CTR. In the feedback loop, the collector-emitter voltage V_{co} is divided by a factor V_{div} before being fed to the current peak comparator (V_{div} = 6 V for the NCP12700). The control voltage V_{co} provided by the compensator in a CCM current-mode converter controls the primary peak current setpoint, and thus its level depends on the converter output power. For full-load, the control voltage will be at the maximum value, and as the load reduces, the control voltage will be lower. Note that the CTR varies slightly with V_{ce}.

The following expression can be used to estimate the control voltage fed to the comparator in a peak current-mode Flyback converter:

$$V_c = V_{div} \cdot \left[\frac{D}{F_{sw}} \cdot \left(S_a + \frac{V_{in} \cdot R_s}{2 \cdot L} \right) + \frac{V_{out} \cdot I_{out} \cdot R_s}{D \cdot V_{in}} \right] \tag{25}$$

Taking $V_{in(nom)}$ = 48 V, S_a = 55 kV/s, (middle of the range of S_a = 33 kV/s to 80 kV/s) and full load I_{out} = 2.5 A, it is obtained:

$$V_c = 2.71 \text{ V}$$

This generates a steady-state collector current of:

$$I_c = \frac{V_{dd} - V_c}{R_c} = 0.46 \text{ mA} \tag{26}$$

A WL-OCPT optocoupler from binning A is selected for the design, and the resulting CTR under this bias condition can be measured experimentally using the setup shown in Appendix A. Alternatively, it can be obtained with the LTspice™ simulation fixture shown in Figure 19, thanks to individual SPICE models provided by Würth Elektronik for each binning of the WL-OCPT 817 optocoupler series. In this case, for V_{ce} = 2.7 V, the CTR is 0.71, with an LED current of 0.65 mA and a collector current of 0.46 mA.
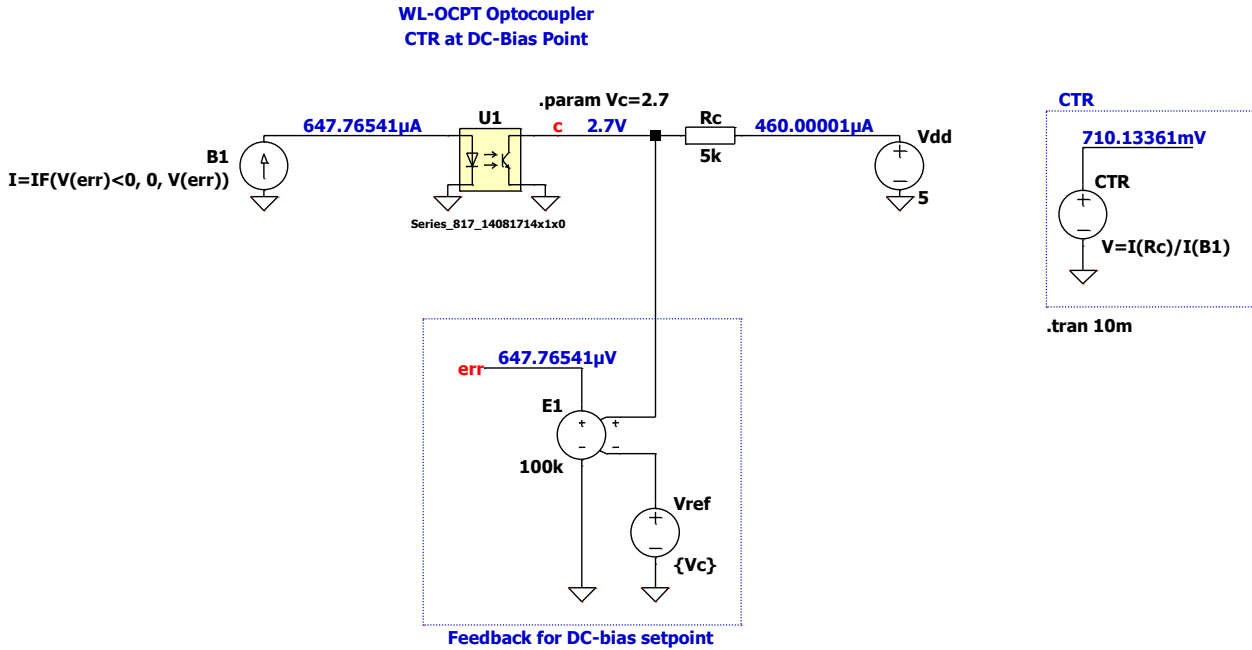
Figure 19: SPICE simulation for obtaining CTR with SPICE model of WL-OCPT 817 A (LTspice™)

Note that these SPICE models consider a CTR near the average of the tolerance range of the respective binning at DC-bias conditions of V_{ce} = 5 V and I_F = 5 mA (in this case for binning 'A' this is $CTR_n \approx 1.2$). The relative CTR for this DC-bias condition is:

$$CTR_{rel} = \frac{CTR}{CTR_n} = \frac{0{,}71}{1.2} \approx 0.6 \tag{27}$$

Since the CTR only changes slightly with collector-emitter voltage (as long as the phototransistor stays in the active region of operation), a similar CTR value of 1.2 for V_{ce} = 5 V and V_{ce} = 2.7 V at I_F = 5 mA can be approximated. Figure 20 shows that the relative CTR vs LED current curves for different binnings do not differ notably below an LED current of 5 mA, however, as the optocoupler phototransistor starts to operate close to the saturation region (V_{ce} below 0.5 V), more difference in the curves will be observed. With this, based on Figure 20, an LED current of 0.65 mA would correspond to a relative CTR of around 0.55 considering a device from bin A. Relative CTR curves help to estimate the absolute CTR of a device when its CTR value at the test DC-bias conditions deviates considerably from the average value of the binning.

To the obtained absolute CTR value of 0.71, the production tolerance spread of the binning 'A' must be added. A minimum and maximum CTR of 0.8 and 1.6 corresponds to a deviation of ±30% from the average CTR of 1.2. The range in this design is then:

$$CTR_{tol\_min} = 0.71 \cdot 0.7 \approx 0.49$$

$$CTR_{tol\_max} = 0.71 \cdot 1.3 \approx 0.91$$

Note that the relative CTR curve in previous Figure 18 considers an operating temperature of 25°C, but the CTR also varies with ambient temperature as shown in Figure 21. Considering a temperature range of -20°C to 85°C, the minimum CTR value calculated above must be multiplied by a factor of 0.85 (@T_a = 85°C), and the maximum by a factor of 1 (@T_a = 10 to 30°C), obtaining the new CTR range:

$$CTR_{tol\_temp\_min} = 0.49 \cdot 0.85 \approx 0.42$$

$$CTR_{tol\_temp\_max} = 0.91 \cdot 1 = 0.91$$

The minimum CTR value at start-of-life is in this case:
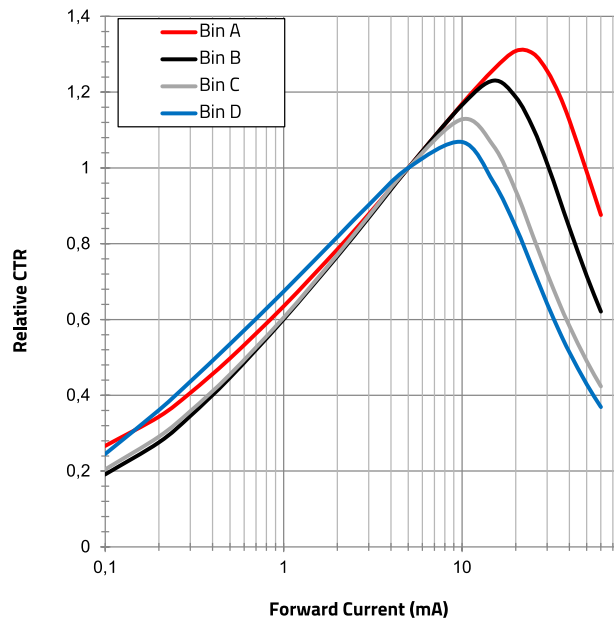
$$CTR_{min\_sol} = 0.42$$

Figure 20: WL-OCPT 817 Series: Relative CTR vs. LED forward current (at V_{ce} = 5 V)
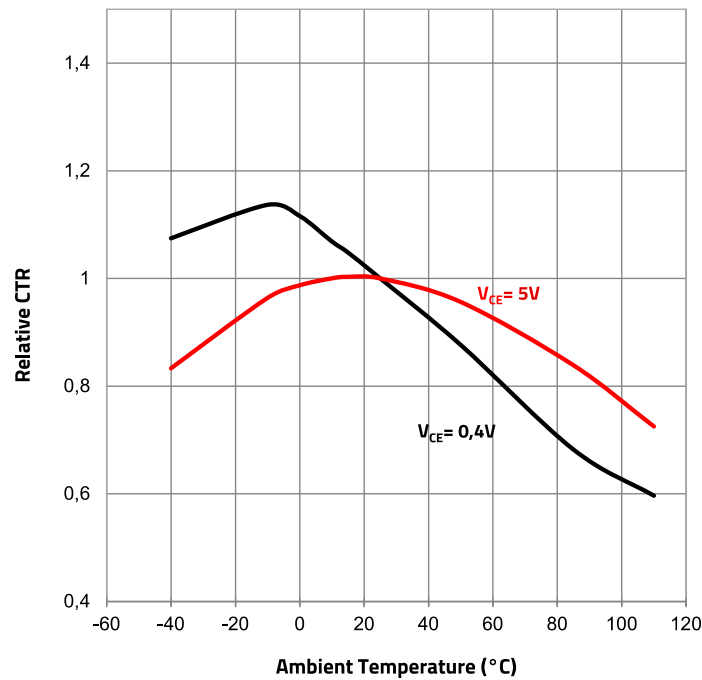

Figure 21: WL-OCPT 817 series - Relative CTR vs. Ambient Temperature curve

Minimum CTR at end-of-life

The optocoupler CTR also reduces with operating time. This is caused mainly by degradation of the LED with the corresponding reduction in emission efficiency, as the LED generates fewer photons for the same forward current. The rate of degradation is directly proportional to the LED operating temperature, and in turn, to the LED forward current. The Application Note in

reference [13] provides guidance to estimate the expected CTR reduction for a set operating condition. In this design, considering a maximum temperature of 80°C and LED current of 0.65 mA, based on the test curves [13] for 20 years' operating time the CTR would degrade less than 5%. This however considers an LED current of 5 mA, which is much higher than the maximum in this design (0.2 mA ≤ I_{LED} ≤ 0.42 mA). Although the CTR degradation for this design specification can be neglected, for the sake of the example, a degradation of 5% is considered:

$$CTR_{eol} = CTR_{min\_sol} \cdot 0.95 = 0.4$$

An absolute minimum current transfer ratio of CTR_{min} = 0.35 is considered, adding some extra margin.

LED resistor calculation

From previous E.24, considering V_z = 9 V (see next for details), V_{ce_sat} = 0.2 V [11] and V_f = 0.81 V, it is obtained:

$$R_{LED\_max} = \frac{(V_z - V_f - V_{ref\_TL431}) \cdot CTR_{min} \cdot R_c}{(V_{dd} - V_{ce\_sat} + I_{b\_TL431} \cdot CTR_{min} \cdot R_c)} = 1.18 \text{ k}\Omega$$

A slightly lower standard value of 1 kΩ is selected.

$$R_{LED} = 1 \text{ k}\Omega$$

Note that the resistor value does not have any influence on the LED current, which is set only by the collector current and the CTR when the converter is operating in closed-loop, since the collector-emitter voltage is set by the required duty-cycle, which in turn is set by the input voltage and load current.

The AC decoupling Zener supply

The components R_z, D_z and C_z form a simple Zener regulated supply, whose main function is to provide a DC voltage to the LED anode which is AC-decoupled from the converter output voltage. This way, it is ensured that the LED current is only AC-modulated by the TL431 cathode voltage. Otherwise, the LED current would also become AC-modulated by the output voltage variations itself, which would place further constraints in choosing the LED resistor value (see [3] for more details).

The Zener voltage needs to be chosen high enough to provide a wide dynamic range to control the LED current and reduce power dissipation in R_z, but at the same time low enough to keep power dissipation in the Zener diode low. A Zener voltage of 70 to 80% of the output voltage (V_{out}=12 V) is considered in this case as a good compromise:

$$V_z = 0.8 \cdot V_{out} = 9.6 \text{ V} \tag{28}$$

A device with standard voltage V_z = 9.1 V is selected.

The maximum value of the Zener resistor (R_z) is limited by the maximum current across the LED resistor plus the bias current of the Zener diode (I_{b_Zener}), selected in this case as 2 mA in order to reduce its impedance and improve with its AC filtering, as follows:

$$R_z \leq \frac{(V_{out} - V_z)}{(I_{b\_Zener} + I_{b\_TL431} + I_{LED\_max})} = \frac{(V_{out} - V_z)}{I_{Rz}} = \frac{2.9 \text{ V}}{5 \text{ mA}} = 580 \text{ }\Omega \tag{29}$$

A standard value of 470 Ω is selected. The power dissipation in the resistor is:

$$P_{Rz} = I_{Rz}^2 \cdot R_Z = 25 \text{ μA} \cdot 470 \text{ }\Omega = 11.75 \text{ mW} \tag{30}$$

The maximum power dissipation in the Zener diode happens when the LED current is zero:

$$P_{z\_max} = (I_{Rz} - I_{b\_TL431\_min}) \cdot V_Z = 3 \text{ mA} \cdot 9.1 \text{ V} = 27 \text{ mW} \tag{31}$$

The calculated values are acceptably low for good efficiency and thermal management considerations.

The resistive divider

The resistors R_1 and R_{low} set the output voltage to the desired value, based on the reference voltage of the TL431. Setting R_{low} = 10 kΩ, then:

$$R_1 = \frac{(V_{out} - V_{ref}) \cdot R_{low}}{V_{ref}} = \frac{(12\ V - 2.5\ V) \cdot 10\ k\Omega}{2.5\ V} = 38\ k\Omega \tag{32}$$

A value of 38.3 kΩ is selected.

5.3 Compensator components design

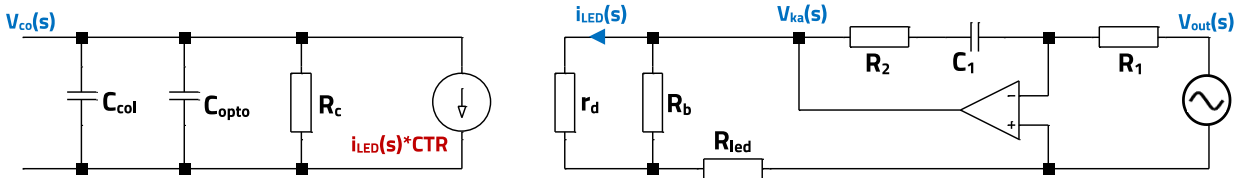For AC-analysis, the compensator circuit from previous Figure 13 can be replaced by the AC schematic of Figure 22.

Figure 22: Equivalent AC circuit for the Type 2 compensator with TL431 and WL-OCPT Optocoupler

In the AC circuit model, the TL431 is modelled like an error amplifier, producing an AC voltage $V_{ka}(s)$ which modulates the LED current. In this regard, the LED dynamic resistor (r_d) is also included in the model. Although its value is typically very small, it increases as the LED current reduces, causing a higher portion of the LED current to flow through the bias resistor R_b instead, reducing with it the compensator gain. Note that the capacitance C_{opto} is the parasitic collector-emitter capacitance of the optocoupler phototransistor.

The transfer function of a Type 2 compensator like that of figure 13 features a zero (ω_z), a pole (ω_p), and an origin pole (ω_{po}):

$$C(s) = \frac{V_{co}(s)}{V_{out}(s)} = -G_m \cdot \frac{\left(1 + \frac{\omega_z}{s}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \tag{33}$$

Where $G_m = \omega_{po}/\omega_z$. From the circuit of Figure 22, the following transfer function expression is obtained:

$$C(s) = \frac{V_{co}(s)}{V_{out}(s)} = -\left(\frac{R_c \cdot CTR}{R_{LED}} \cdot \frac{R_2}{R_1}\right) \cdot \frac{\left(1 + \frac{1}{sR_2C_1}\right)}{\left(1 + sR_c\left(C_{col} + C_{opto}\right)\right)} \tag{34}$$

Considering $s = j\ \omega = j\ 2\ \pi\ f$, it is obtained:

$$\text{midband Gain} = |G_m| = \frac{R_c \cdot CTR}{R_{LED}} \cdot \frac{R_2}{R_1} \tag{35}$$

$$f_z = \frac{1}{2 \cdot \pi \cdot R_2 \cdot C_1} \tag{36}$$

$$f_p = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_{col} + C_{opto})} \tag{37}$$

Note that the CTR parameter in the compensator AC circuit model and in the midband gain expression (E.35) corresponds to the small-signal CTR of the optocoupler, which in this case is slightly higher than the DC-CTR value calculated. Note however that the DC-CTR value will still be considered for the following compensator design steps as an approximation.

Figure 23 shows the typical frequency response characteristic of a Type 2 compensator. If the zero is located at a lower frequency than the pole, then exactly at a frequency equal to the geometric means of the two frequencies ($f_g=\sqrt{(f_z \cdot f_p)}$), the gain equals the midband gain G_m. This is also the frequency of the maximum phase boost of the compensator. The further apart the pole and zero are, the higher the phase boost provided, up to a maximum of 90°.

Based on this, if the pole-zero geometric means frequency is set at the target crossover frequency of the open-loop transfer function ($f_g = f_c$), then the midband gain of the compensator can be simply set to offset the gain of the plant at f_c, and the zero and pole frequencies are placed symmetrical to f_c and far enough apart to provide the phase boost necessary to meet the phase margin specification. This compensation procedure is known as 'k-factor' [3][4].
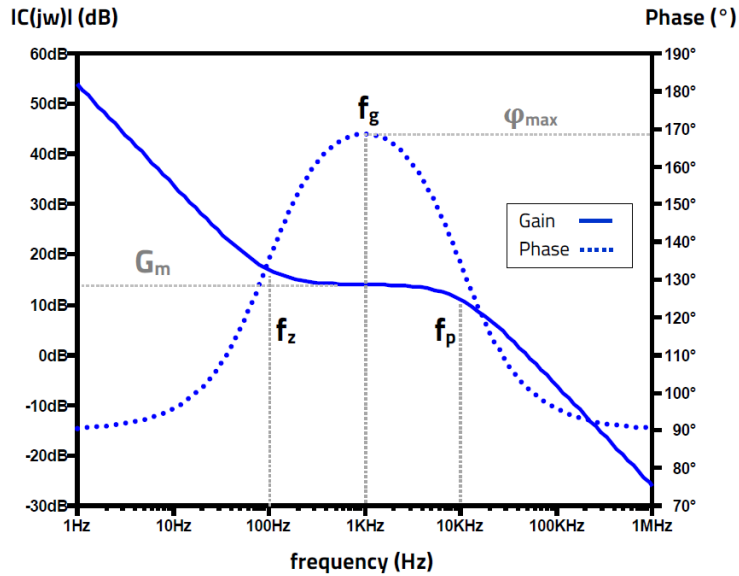
Figure 23: Type-2 compensator: Frequency response example (LTspice™ simulation)

In this compensator circuit, the midband gain directly depends on the CTR (E.35), so we can advance that any CTR variations will cause a change in the midband gain and in turn, a shift in the crossover frequency of the open-loop transfer function, from which additionally the phase margin will be affected. This shows the importance of knowing not only the minimum CTR, but also the full range of CTR variation. Note that the small-signal CTR follows the variations of the DC-CTR over the full current range of this application (below 1 mA). It is also observed that the collector-emitter parasitic capacitance of the optocoupler phototransistor (C_{opto}) sets the pole frequency of the compensator, together with any added capacitance (C_{col}).

From previous section 4, the compensator specification is recalled as:

$$f_c = 10 \text{ kHz}$$

$$|C(f_c)| = 4.12 = +12.3 \text{ dB}$$

$$\varphi_{comp\_lead}(f_c) = +76.4°$$

Since values of CTR, R_c, R_{LED} and R_1 are already set for DC-biasing purposes, R_2 is calculated to set the required midband gain:

$$R_2 = \frac{R_1 \cdot R_{LED} \cdot |G_m|}{R_c \cdot CTR_{nom}} = \frac{38k \cdot 1k \cdot 4.12}{5k \cdot 0.71} = 44.1 \text{ k}\Omega \tag{38}$$

A standard value of $R_2 = 44.2 \text{ k}\Omega$ is selected.

To obtain a phase lead of +76° at 10 kHz, the zero and the pole frequencies are calculated as follows [3]:

$$f_p = \left(\tan\left(\varphi_{comp\_lead} \right) + \sqrt{\tan^2\left(\varphi_{comp\_lead} \right) + 1} \right) \cdot f_c \tag{39}$$

$$f_z = \frac{f_c^2}{f_p} \tag{40}$$

which yields $f_p = 83.25 \text{ kHz}$ and $f_z = 1.2 \text{ kHz}$.

The capacitor C_1 is calculated from previous E.36 to set the zero at the required frequency:

$$C_1 = \frac{1}{2 \cdot \pi \cdot R_2 \cdot f_z} = 3 \text{ nF}$$

A standard value of $C_1 = 3.3 \text{ nF}$ is selected, with a zero frequency slightly lower at $f_z \approx 1.1 \text{ kHz}$.

The capacitance at the compensator output necessary to set the pole frequency is (E.37):

$$C_{col} + C_{opto} = \frac{1}{2 \cdot \pi \cdot R_c \cdot f_p} = 0.38\ \text{nF}$$

with:

$$C_{col} = 0.38\ \text{nF} - C_{opto}$$

It is observed that, if the optocoupler parasitic capacitance is higher than 0.38 nF in this case, then the pole cannot be set at the target frequency of 83.25 kHz.

06. OPTOCOUPLER POLE LIMITATION AND SOLUTIONS

The collector-emitter parasitic capacitance of the optocoupler (C_{opto}) and in turn the pole frequency varies slightly with the collector-emitter voltage (V_{ce}). The lower the collector-emitter voltage, the lower the pole frequency (due to higher C_{opto}). For this design, taking V_{ce} = 2.7 V as calculated before for full-load condition, the pole frequency of the WL-OCPT 140817140110 device has been measured with the setup shown in Appendix B. Figure 24 shows results of one of the samples measured. Out of a total of 20 units, the measured pole frequency was found between 24.2 and 25 kHz. Taking f_p = 24.6 kHz in the middle of the range, this corresponds to a parasitic capacitance of:

$$C_{opto} = \frac{1}{2 \cdot \pi \cdot R_c \cdot f_{p\_opto}} = 1.3\ \text{nF} \tag{41}$$

	Frequency	Mag (dB)	Phase (deg)
Low Frequency	100 Hz	-1,648 dB	-163,306 m°
Pole Frequency	24,64 kHz	-4,648 dB	-46,769 °
Delta Py-Ly	24,54 kHz	-3 dB	-46,606 °
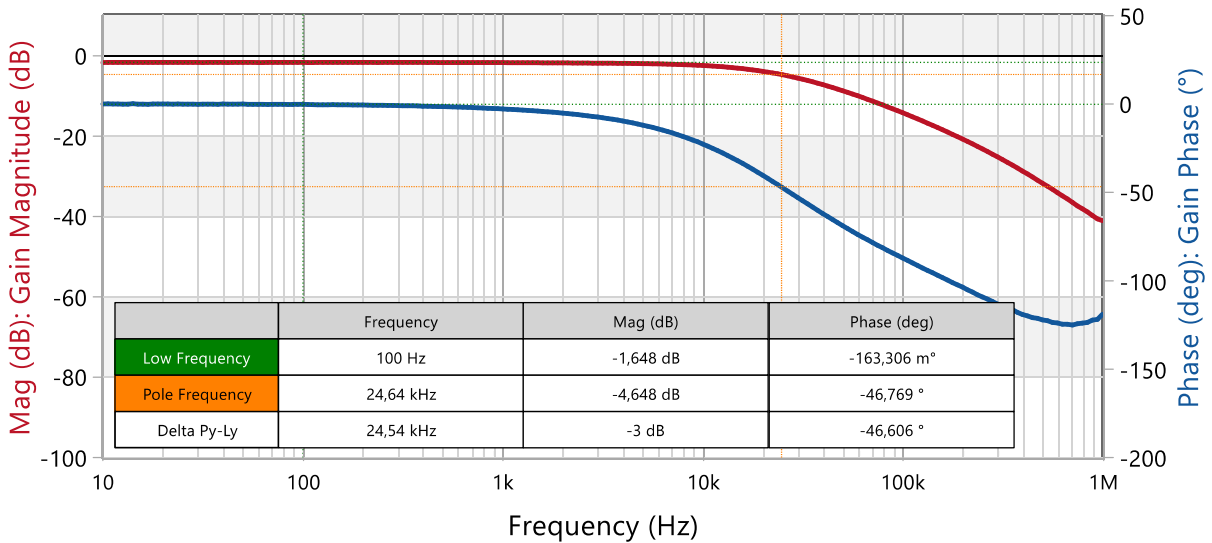
Figure 24: Measurement result for WL-OCPT 817 Bin A pole frequency (Bode100™)

Measurements were also made for V_{ce} = 2 V, resulting in a slightly lower pole frequency in the range of 22.9 to 23.7 kHz.

Note that if a WL-OCPT device from another binning with higher CTR were selected (e.g. Bin 'B' or 'C'), the optocoupler pole frequency will be lower. For the same DC-Bias conditions as considered here, samples from the Bin 'B' showed a pole frequency of around 18 kHz, whereas for the Bin 'C', it was around 12.5 kHz. The reason for this is the mutual dependence of the CTR and Copto. A higher CTR can be achieved, for example, by increasing the base-collector area of the output phototransistor so that to increase its sensitivity to the oncoming photonic energy. This however results in a higher parasitic capacitance and a lower optocoupler pole frequency.

In E.41, it is observed that C_{opto} is higher than the maximum value of 0.38 nF required to set the compensator pole at 83.25 kHz in this design.

6.1 Solution 1: Select a lower crossover frequency

A typical solution to the optocoupler limitation is to reduce the target crossover frequency. However, special attention should be paid to the transient response, since a lower crossover frequency of the open-loop transfer function causes the control loop to react more slowly to transients.
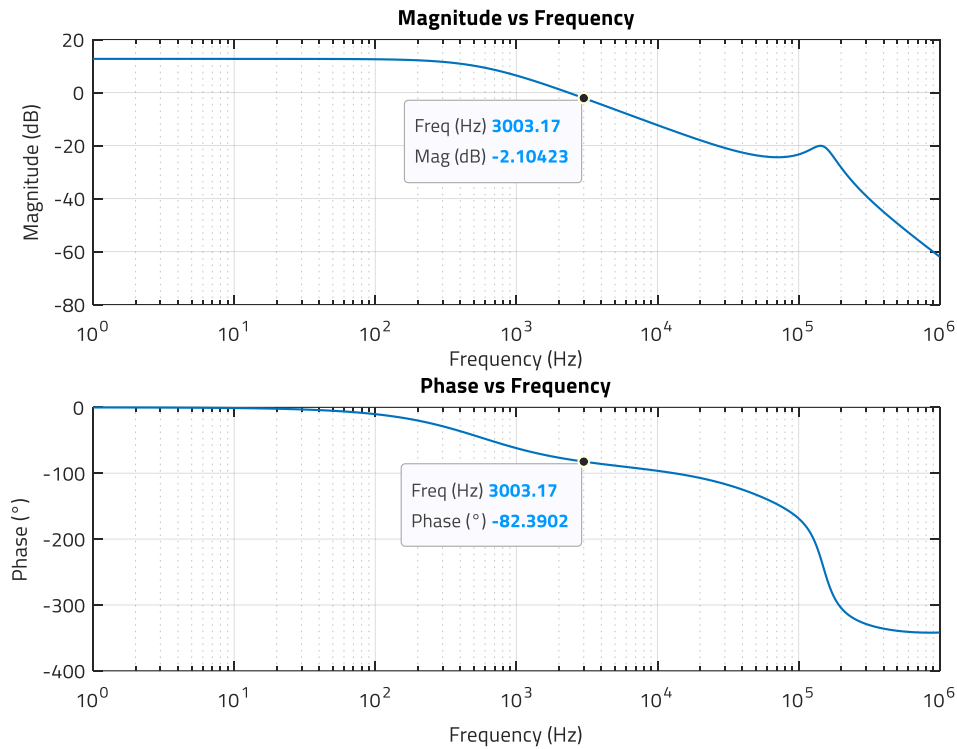
Figure 25: Magnitude (dB) and phase (°) of plant transfer function at f_c = 3 kHz with S_{a_min} = 30 kV/s (MATLAB™)

Selecting f_c = 3 kHz, from the plant magnitude and phase in Figure 25, the requirements for the compensator are:

$$|C(f_c)| = +2.1 \text{ dB}$$

$$\varphi_{comp\_lead}(f_c) = 70° - 90° - 83.2° \approx 62°$$

The required zero and pole frequencies are recalculated from E.39 and E.40:

$$f_z = 748 \text{ Hz}$$

$$f_p = 12.03 \text{ kHz}$$

Compensator component values are also recalculated:

$$R_2 = 13.8 \text{ k}\Omega \text{ (14 k}\Omega \text{ is selected)}$$

$$C_1 = 15.4 \text{ nF (15 nF is selected)}$$

The zero frequency with the selected values is f=758 Hz

$$C_{col} + C_{opto} = 2.6 \text{ nF}$$

$$C_{col} = 1.3 \text{ nF (1 nF is selected)}$$

$$C_{col} + C_{opto} = 2.3 \text{ nF}$$

The pole frequency with the selected C_{col} value is slightly higher at f_p = 13.8 kHz.

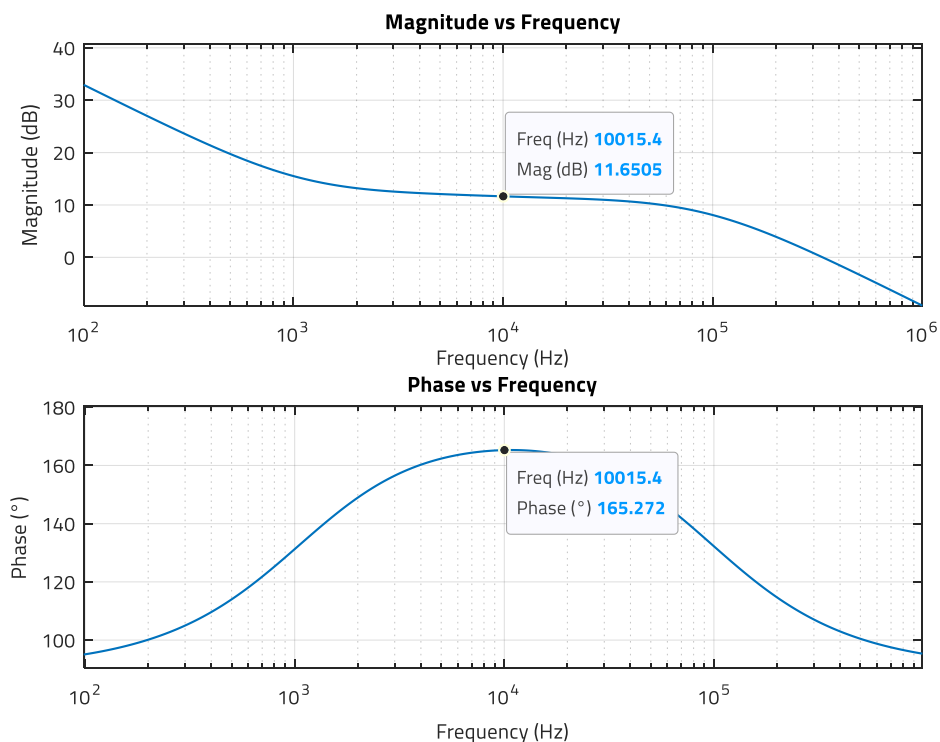With these values, the compensator frequency response of Figure 26 is obtained.
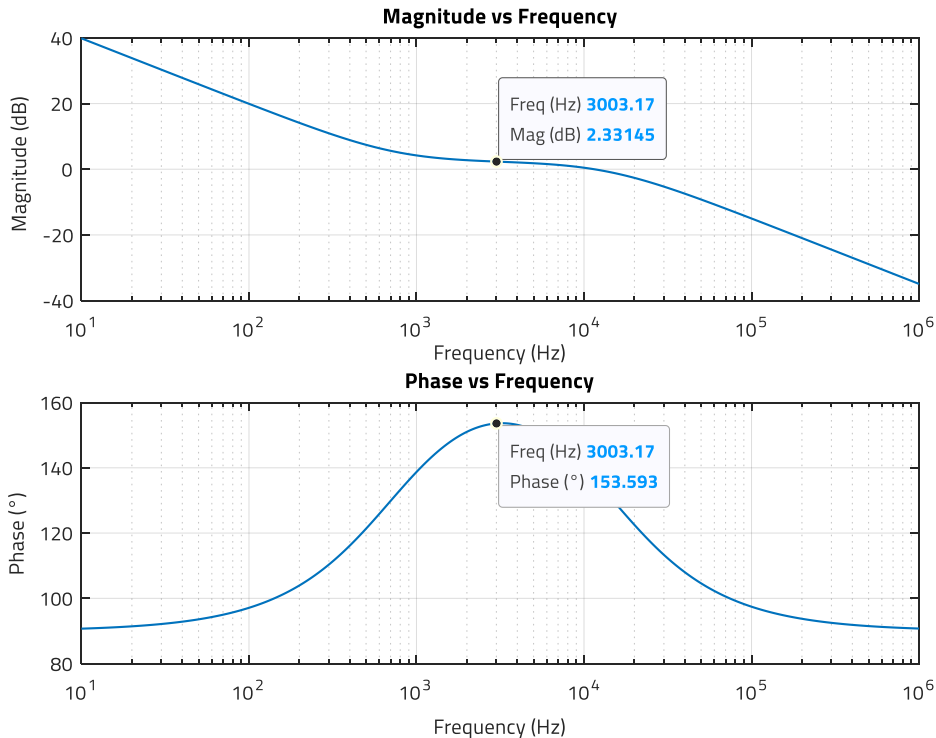
Figure 26: Magnitude (dB) and phase (°) of compensator for solution-1 (MATLAB™)

It is observed how at the target f_c = 3 kHz, the gain is around 2.3 dB and the phase boost: 153.5° - 90° = 63.5°. These very close but not exact values to the requirement are the result of using standard available values for the components, instead of those theoretically calculated.

6.2 Solution 2: Add a zero to cancel the optocoupler pole. Add a pole for the compensator

If the crossover frequency cannot be reduced, a possible solution is to add both a zero and a pole to the system. The zero will be set at the optocoupler pole frequency to cancel its effect. The pole is set at the target pole frequency of the compensator.

With this, the limitation from C_{opto} is eliminated and the target crossover frequency can be achieved. A resistor (R_3) and a capacitor (C_3) in parallel with R_1 create the additional pole and zero, as shown in Figure 27.

This configuration corresponds, in fact, to a Type 3 compensator, but since the effects of the added zero and the optocoupler pole mutually cancel each other, the system effectively provides a Type 2 compensator response, with a zero, a pole and a midband gain.

Note that the added zero can compensate the optocoupler pole directly, or an additional capacitance C_{col} can be added to shift the pole at a lower frequency range, and then cancel it there. This helps to reduce the impact of the small variations in the optocoupler pole frequency.

Adding C_{col} = 3.3 nF, the pole frequency is shifted to (E.37):

$$f_{p1} = f_{z2} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_{col} + C_{opto})} = 6.92 \text{ kHz}$$

The pole is placed at the required frequency previously calculated (E.39) (f_{p2} = 83.25 kHz), and R_3 is calculated to set the zero [3]:

$$R_3 = R_1 \cdot \frac{f_{z2}}{(f_{p2} - f_{z2})} = 3.47 \text{ k}\Omega \tag{42}$$
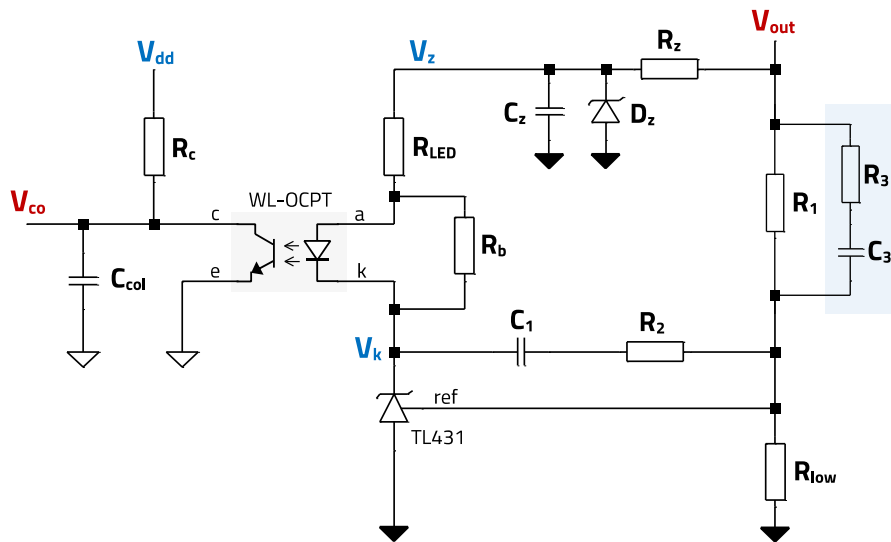
Figure 27: Type 3 compensator configuration with TL431 and WL-OCPT optocoupler

A value R_3 = 3.6 kΩ is selected. The capacitor C_3 is calculated to set the pole [3]:

$$C_3 = \frac{1}{2 \cdot \pi \cdot R_3 \cdot f_p} = 0.53 \text{ nF} \tag{43}$$

A value of C_3 = 0.47 nF is selected. With this, the compensator frequency response obtained is:

Figure 28: Magnitude (dB) and phase (°) of compensator for solution 2 (MATLAB™)

It is observed how at the target f_c = 10 kHz, the gain provided is around 11.65 dB and the phase boost: 165.3° - 90° = 75.3°.

07. OPEN-LOOP RESPONSE: PHASE AND GAIN MARGINS

For solution-1 (Figure 29), it is observed a crossover frequency of 3.06 kHz and a phase margin of around 71°. The gain margin is around 25 dB, far higher than the minimum recommended of 6 dB. Regarding solution 2 (Figure 30), it is observed a crossover frequency of around 9.3 kHz and a phase margin of 69.2°, nearly 70°. The gain margin is around 15 dB, showing the importance of damping the resonant double-pole.
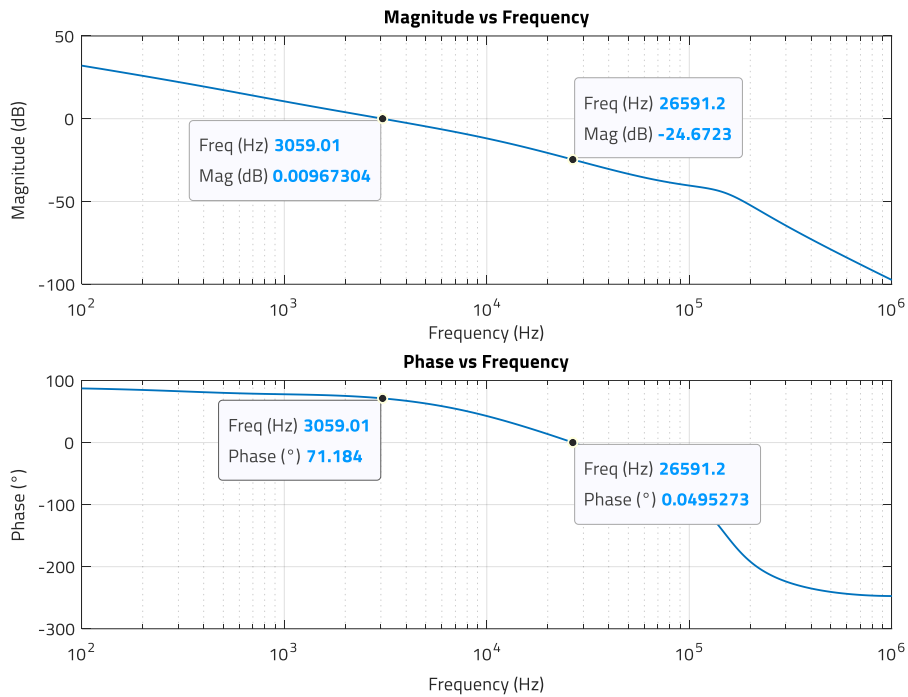
Figure 29: Magnitude (dB) and phase (°) of open-loop transfer function for compensator solution 1 (MATLAB™)
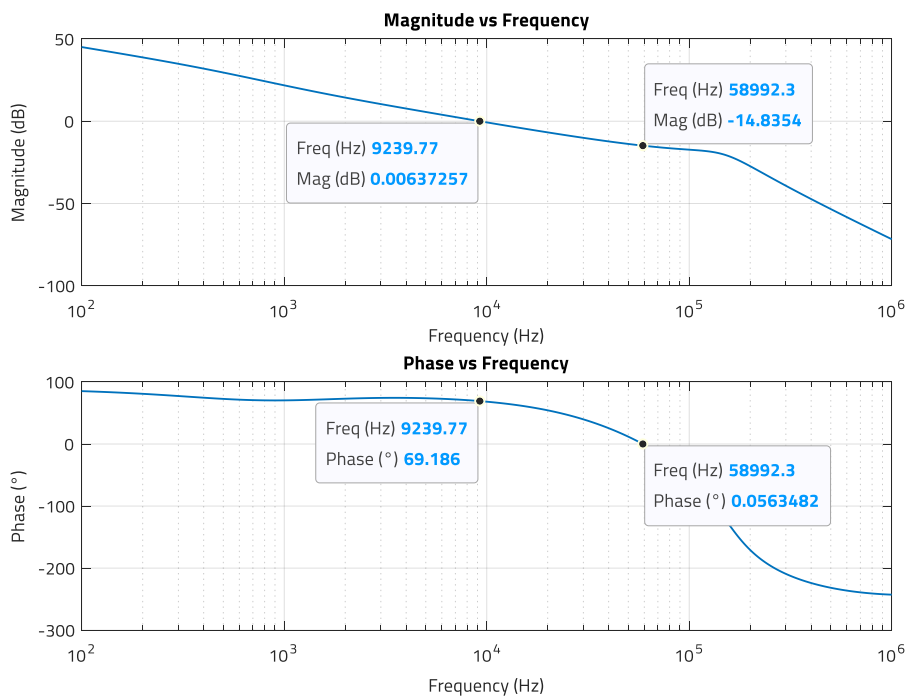
Figure 30: Magnitude (dB) and phase (°) of open-loop transfer function for compensator solution 2 (MATLAB™)

08. TRANSIENT RESPONSE COMPARISON

A higher open-loop crossover frequency (solution-2) provides a higher bandwidth for the closed-loop system. A higher bandwidth means that the loop will react faster to correct the output voltage after any transient deviations from the regulated value. This can be appreciated in Figure 31, which compares the transient response of both solutions to a load current step from 2 to 2.5 A with a slew-rate of 1 A/us. Although the transient response is 'well-behaved' in both cases without ringing due to the high phase margin of 70°, it is observed how the higher closed-loop bandwidth of solution 2 causes lower overshoot and undershoot as well as shorter settling time due to the faster reaction time. Note that the results were obtained in LTspice™ with a converter using an averaged PWM switch model as proposed by Christophe Basso in [2] (this is the reason for not observing any switching frequency ripple in these waveforms).
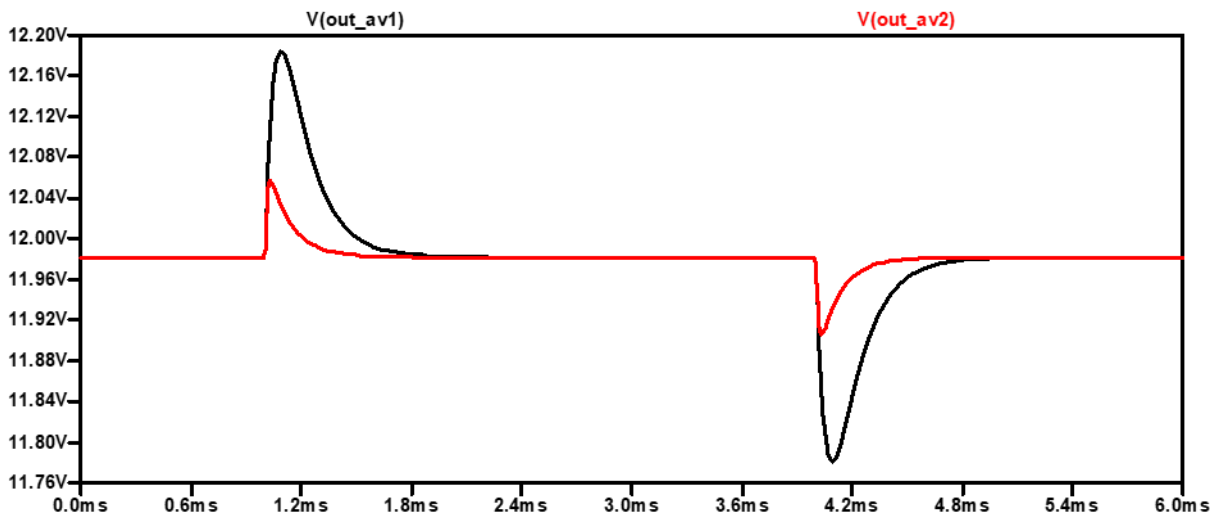
Figure 31: Transient response comparison of solution 1 (black) and 2 (red) (LTspice™ simulation)

09. IMPACT OF OPTOCOUPLER CTR VARIATIONS

Previous expression E.35 shows that the midband gain of the compensator is directly proportional to the optocoupler CTR, as follows:

$$|G_m| = \frac{R_c \cdot CTR}{R_{LED}} \cdot \frac{R_2}{R_1} \tag{44}$$

Theoretically, CTR variations will shift the magnitude curve of the compensator up or down, leaving the phase curve unchanged. In reality, CTR and pole frequency are linked and as the CTR increases, the pole frequency reduces causing a lower phase boost of the compensator. The result is a different crossover frequency of the open-loop transfer function and a different phase margin. For this reason, the system response must be assessed at the CTR limits.

For the case of this design, the CTR range at full-load and minimum input voltage condition is:

$$0.4 \leq CTR \leq 0.91 \tag{45}$$

Fixing the pole frequency for the sake of the example, it can be observed how for the CTR range considered, the midband gain varies as -2.8 dB (CTR = 0.4), 1.47 dB (CTR = 0.65) and 4.2 dB (CTR = 0.9).

The effect of this in the open-loop crossover frequency and phase margin is shown in Figure 32. The crossover frequency is found in the range between 1.75 kHz and 3.7 kHz (target was 3 kHz), and the phase margin in the range 75.2° and 66.5°. In this case, the soft slope of the phase curve ensures that small variations in component parameters do not have a strong impact in the phase margin. Note that in practice, the impact of the pole frequency variations along with CTR can cause a higher phase margin deviation, and this is not shown in Figure 33.
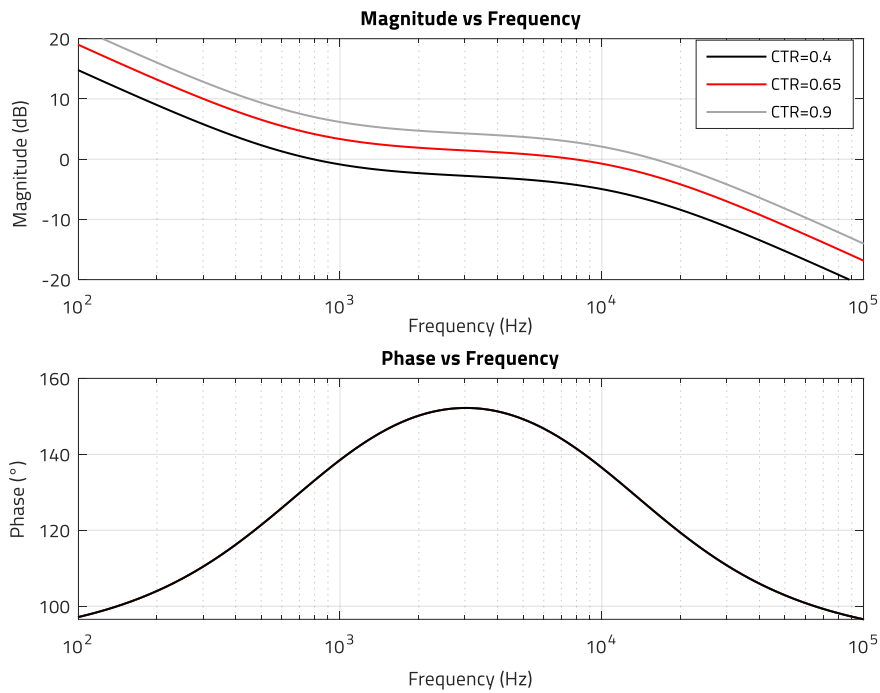
Figure 32: Compensator response versus CTR (MATLAB™)
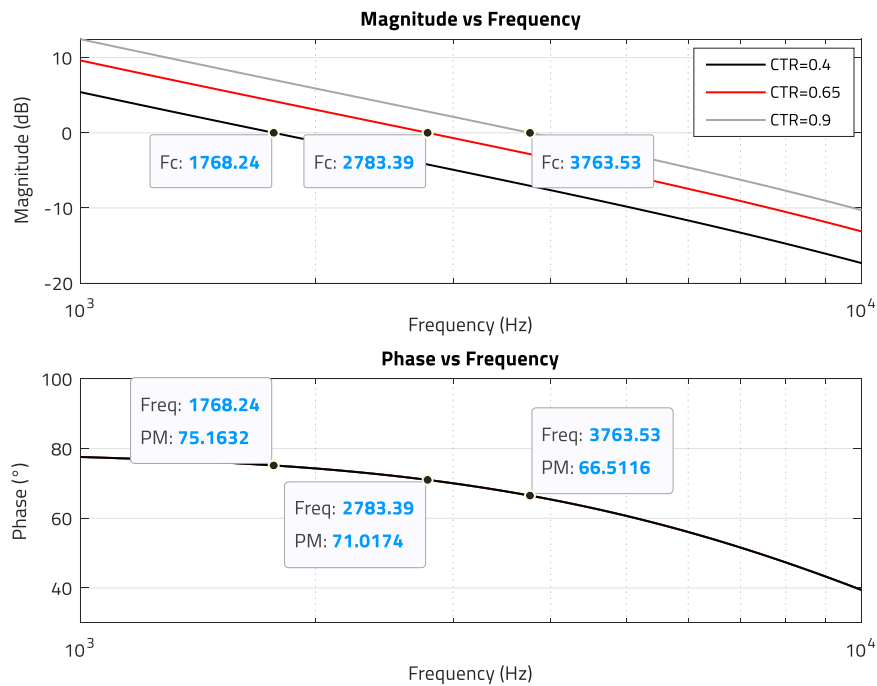
Figure 33: Figure 33. Open-loop transfer function: Fc and PM versus CTR (MATLAB™)

010. DESIGN PROTOTYPE AND EXPERIMENTAL RESULTS

A 30 W Flyback converter prototype based on the specification of section 3 has been built (Figure 34). An optocoupler WL-OCPT from the 817 series and Bin A with a static CTR of 0.71 at the DC-Bias conditions shown in previous section 5.2 was used for the measurements. Note that experimental results in this section are for V_{in_min} = 36 V and full load I_{out} = 2.5 A as designed, but feedback loop stability (phase and gain margins) must still be checked for all other expected operating conditions of the power supply and any required adjustments performed.
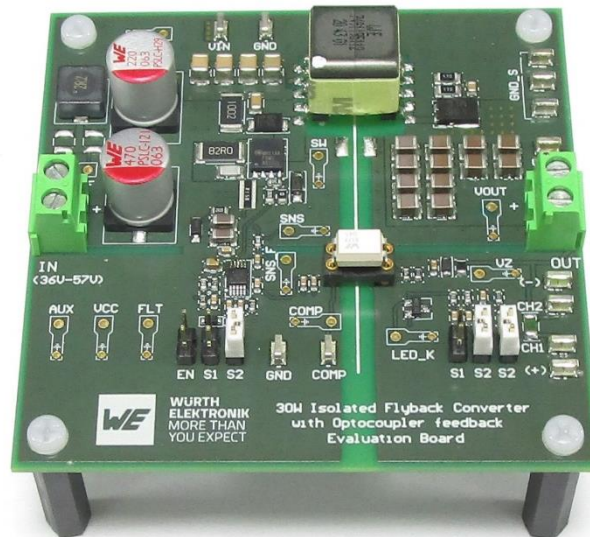
Figure 34: Current-mode Flyback converter with optocoupler board

10.1 Measured Plant Frequency Response

The control-to-output transfer function shows a magnitude and phase in good agreement with analytical results, as shown in Figure 35.

For 3 kHz, analytical results showed gain and phase of -2.1 dB and -82.4°, respectively (Figure 25), close to the measured values of -2.1 dB and -79.4°. For 10 kHz, analytical results were -12.3 dB and -96.3° (Figure 12), also a good approximation to the measured -12.1 dB and -99°.

	Frequency	Mag (dB)	Phase (deg)
Fc_1	3 kHz	-2,101 dB	-79,352 °
Fc_2	10 kHz	-12,123 dB	-98,989 °
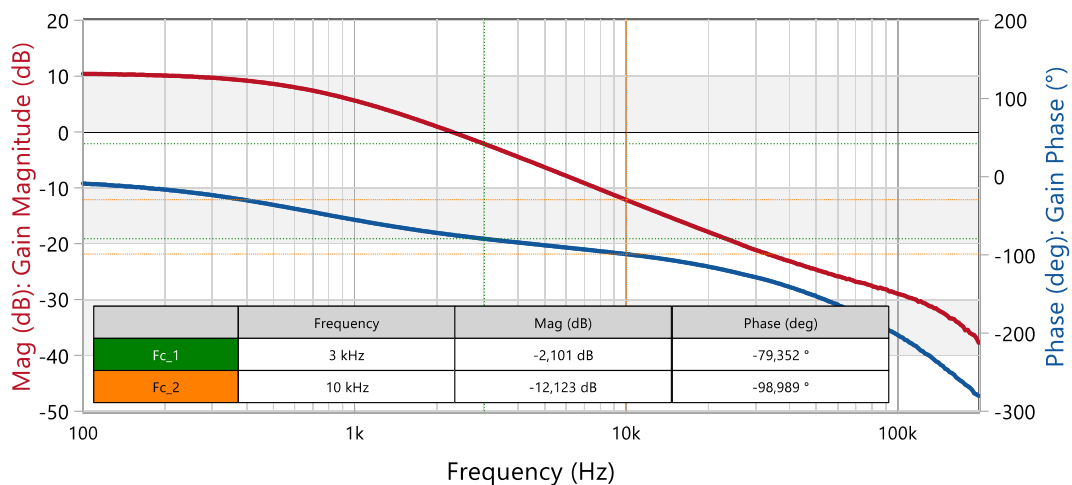
Figure 35: Measured Plant (control-to-output) magnitude and phase frequency response (Vin = 36 V, Iout = 2.5 A) (Bode 100™)

10.2 Results for Compensator Design 1

The compensator in design solution 1 was designed for 2.3 dB gain and 154° phase at 3 kHz (Figure 26). Experimental results show a gain of 2.66 dB and a phase of 155.9° (Figure 36). This is close but not exact since there are different factors affecting the measured values in a real prototype. As previously mentioned, the optocoupler small-signal CTR is slightly higher than the static CTR of 0.71 considered in the design, increasing the measured midband gain. This is partially offset by the reduction in midband gain caused by R_b diverting some current from the optocoupler LED, and the non-ideal AC decoupling provided by the Zener network. The non-exact cancellation of the zero and optocoupler pole can also contribute to differing results.

The open-loop response shows a crossover frequency of 3.2 kHz with a phase margin of 75.5° and a gain margin of 19.6 dB (Figure 37). The phase margin is higher than the 70° targeted due to the addition of the compensator and plant excess phase. Although this is a robust and very stable design, the compensator can be further 'fine-tuned' for example, by reducing C_1 in order to set a higher zero frequency to reduce the compensator phase boost and with it, reduce the phase margin to the target 70°.

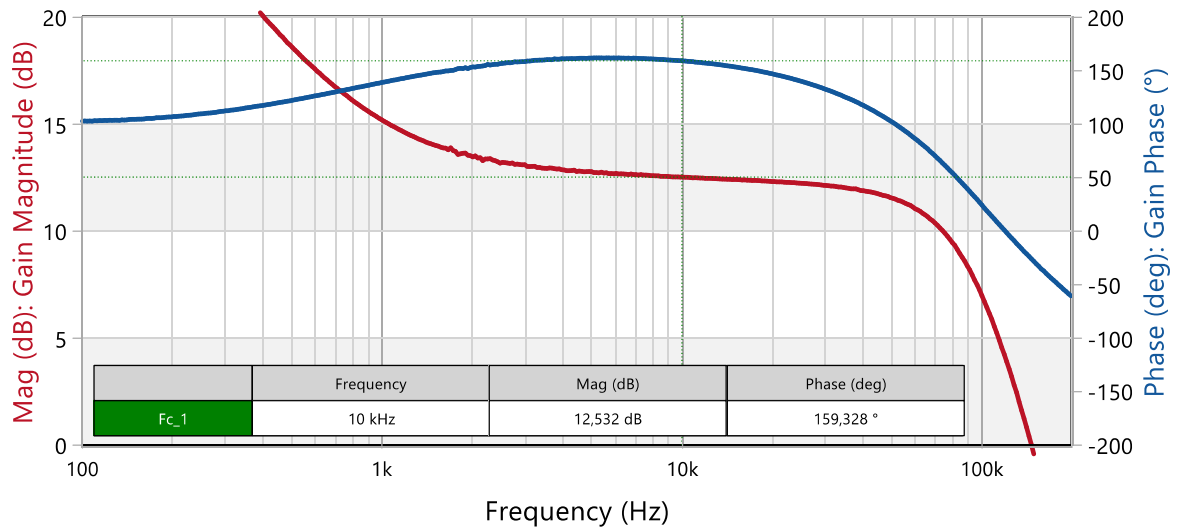|	Frequency	Mag (dB)	Phase (deg)
Fc_1	3 kHz	2,661 dB	155,922 °
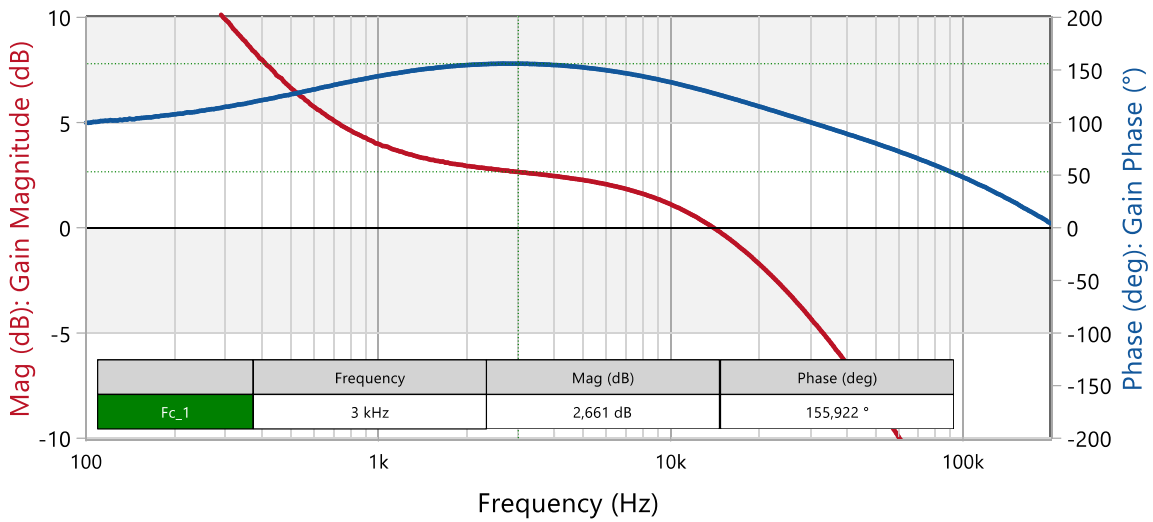
Figure 36: Measured compensator magnitude and phase frequency response for compensator design 1 (Vin = 36 V, Iout = 2.5 A) (Bode100™)

|	Frequency	Mag (dB)	Phase (deg)
Phase Margin	3,234 kHz	0 dB	75,504 °
Gain Margin	20,475 kHz	-19,618 dB	0 °
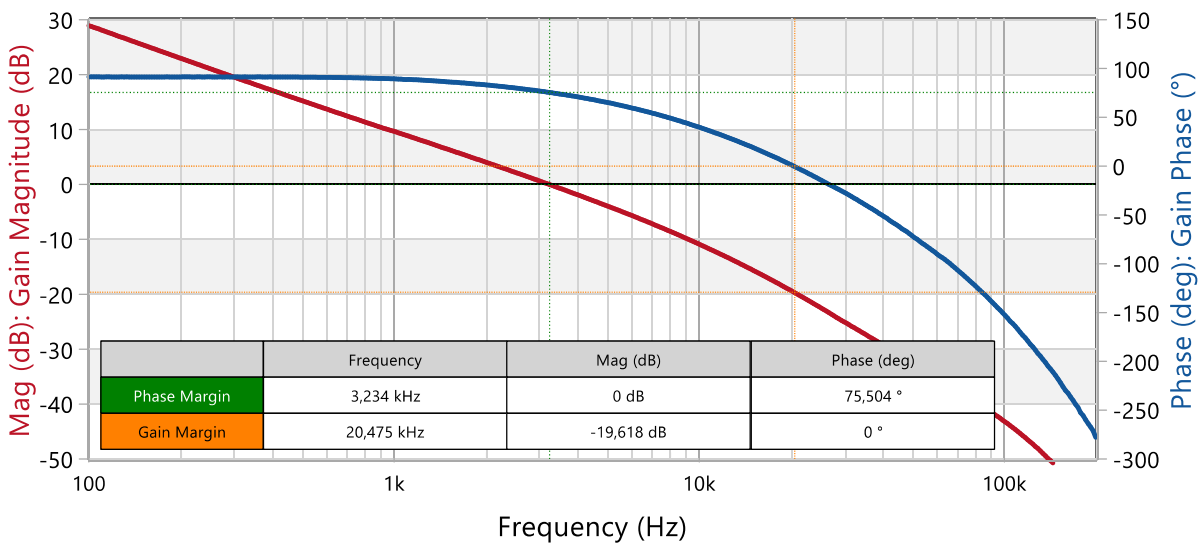
Figure 37: Measured open-loop magnitude and phase frequency response for compensator design 1 (Vin = 36 V, Iout = 2.5 A) (Bode100™)

10.3 Results for Compensator Design 2

The compensator shows a gain of around 12.5 dB and a phase of 159.3° at 10 kHz, and it is observed how it presents a Type 2 characteristic due to the cancellation of the optocoupler pole with the added zero (Figure 38). Analytical results were 11.6 dB and 165° (Figure 28). The cause for the higher gain has been explained in the previous section. A lower phase boost can be caused by a non-ideal cancellation of the zero and the optocoupler pole. However, in this case the main cause seems to be the two additional high-frequency poles appearing at around 100 kHz in the response, as it is observed how the gain rolls off at around -60 dB/dec after the compensator pole and the phase is on its way to -90° (instead of 90°). These poles were not modelled and contribute a small phase lag at 10 kHz. A possible adjustment to increase the compensator phase boost can be to shift the compensator pole at a higher frequency and/or the zero cancelling the optocoupler pole at a lower frequency.

The excess gain provided by the compensator causes an open-loop crossover frequency of 10.2 kHz, higher than the designed result of 9.2 kHz. The phase margin is below the 70° target at around 59° with a gain margin of around 10 dB (figure 39). Although the design is stable, the phase margin can be further increased as explained above. Note that reducing the crossover frequency with a lower compensator midband gain (lower R_2) can help not only to increase the phase margin but also the gain margin in this case.

	Frequency	Mag (dB)	Phase (deg)
Fc_1	10 kHz	12,532 dB	159,328 °

Figure 38: Measured compensator magnitude and phase frequency response for compensator design 2 (Vin = 36 V, Iout = 2.5 A) (Bode100™)

	Frequency	Mag (dB)	Phase (deg)
Phase Margin	10,452 kHz	0 dB	59,061 °
Gain Margin	32,896 kHz	-10,234 dB	0 °
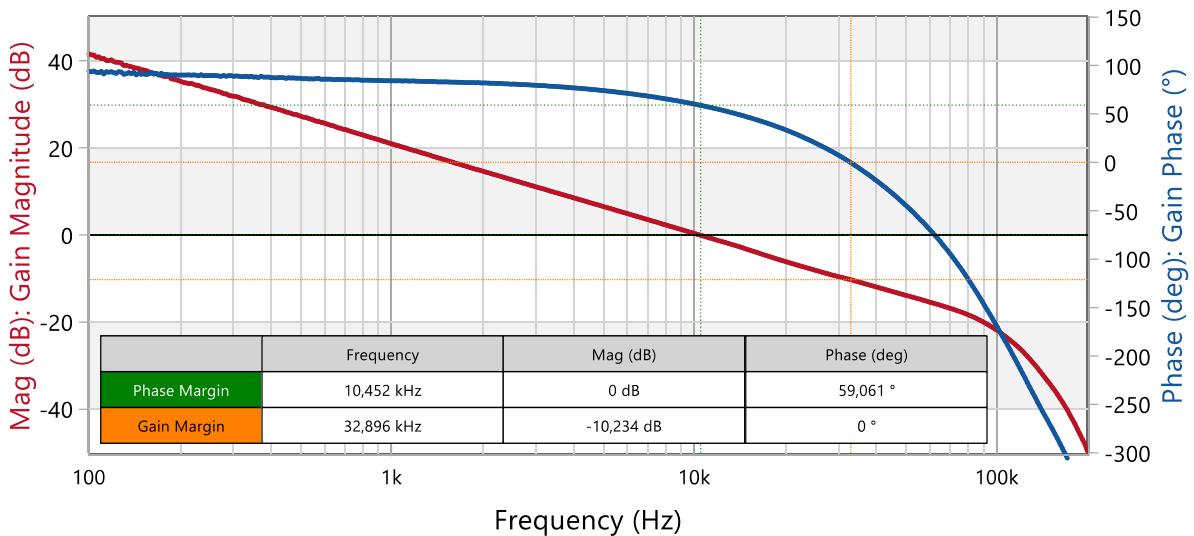
Figure 39: Measured open-loop magnitude and phase frequency response for compensator design 2 (Vin = 36 V, Iout = 2.5 A) (Bode100™)

10.4 Load Transient Response Measurement

Results of the load transient response for both compensator design solutions are shown in Figure 40 (design 1 with f_c = 3.2 kHz and PM = 75.5°) and in Figure 41 (design 2 with f_c = 10.4 kHz and PM = 59°). Note that the axis scale on both oscilloscope captures is the same for direct comparison. Although with a difference in the phase margin, the results are still in line with those from LTspice™ simulation shown in previous Figure 31. As expected, a faster response with lower over- and undershoot as well as a faster settling time is obtained with a higher crossover frequency and a lower phase margin of the open-loop response (design 2).
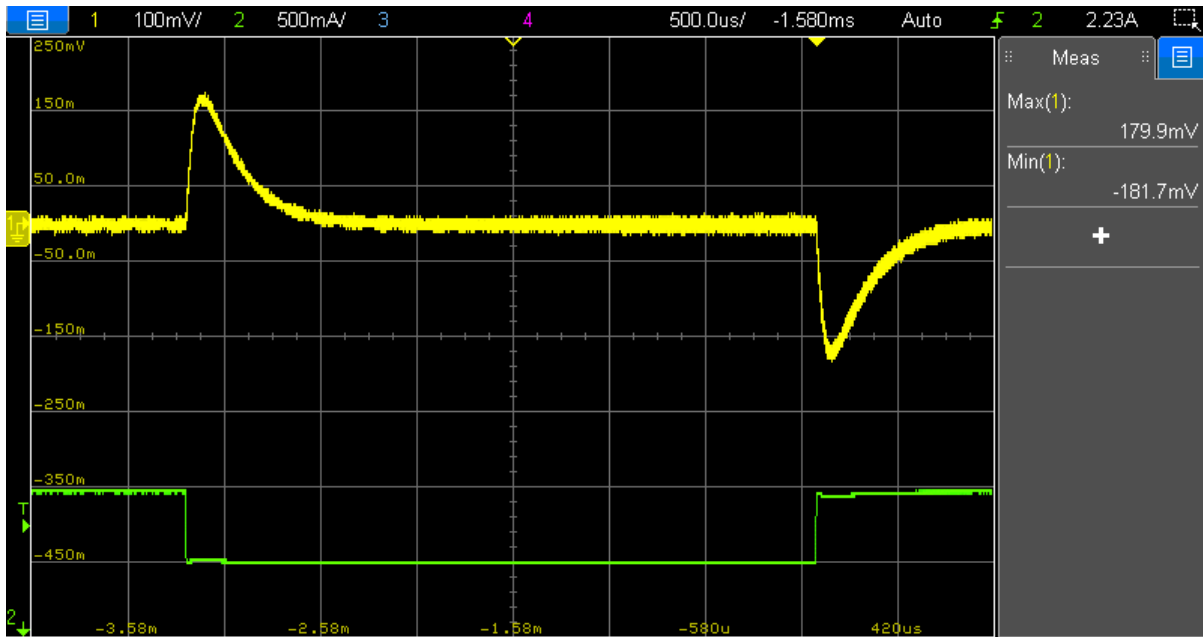
Figure 40: Load transient response for compensator design 1 (Vin = 36 V, fc = 3.2 kHz, PM = 75.5°)) (Iout = 2 A to 2.5 A current step at 1 A/µs)
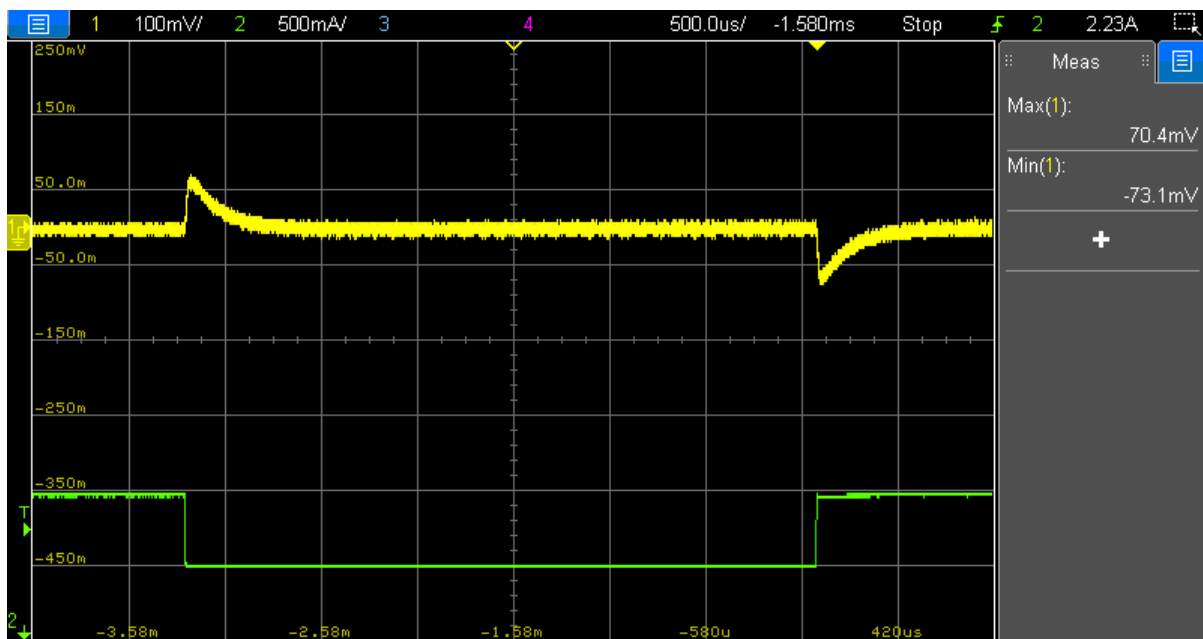
Figure 41: . Load transient response for compensator design 2 (Vin = 36 V, f_c = 10.4 kHz, PM = 59°) (Iout = 2 A to 2.5 A current step at 1 A/µs)

10.5 Results for CTR variation

Experimental results shown previously were obtained with a **WL-OCPT 817** device from bin A and a CTR of 0.7 at the DC-Bias conditions of V_{ce} = 2.7 V and I_c = 0.46 mA. It was seen in previous section 5.2 that the expected maximum CTR for such binning and DC-Bias is 0.9. In order to assess the impact of CTR variation, the converter stability for both compensator designs has been additionally tested with an optocoupler from bin B measuring a CTR of 0.9 at the stated DC-Bias conditions.

It is observed in both cases how the higher CTR causes a higher open-loop crossover frequency as expected, since it increases the compensator midband gain. The phase curve rolls off with increasing frequency causing a reduction of the phase margin. In addition to this, the optocoupler pole frequency decreases with increasing CTR, lowering the compensator phase boost. These are the reasons why the highest CTR represents the worst-case in this particular design.

Although experimental results show a stable control loop, if the compensator had been designed considering the maximum CTR of 0.9 instead of 0.71 as in this document (middle of CTR range), a higher phase margin would be ensured for all other optocoupler devices within the selected binning.

	Frequency	Mag (dB)	Phase (deg)
Phase Margin	4,215 kHz	0 dB	67,799 °
Gain Margin	18,713 kHz	-17,066 dB	0 °
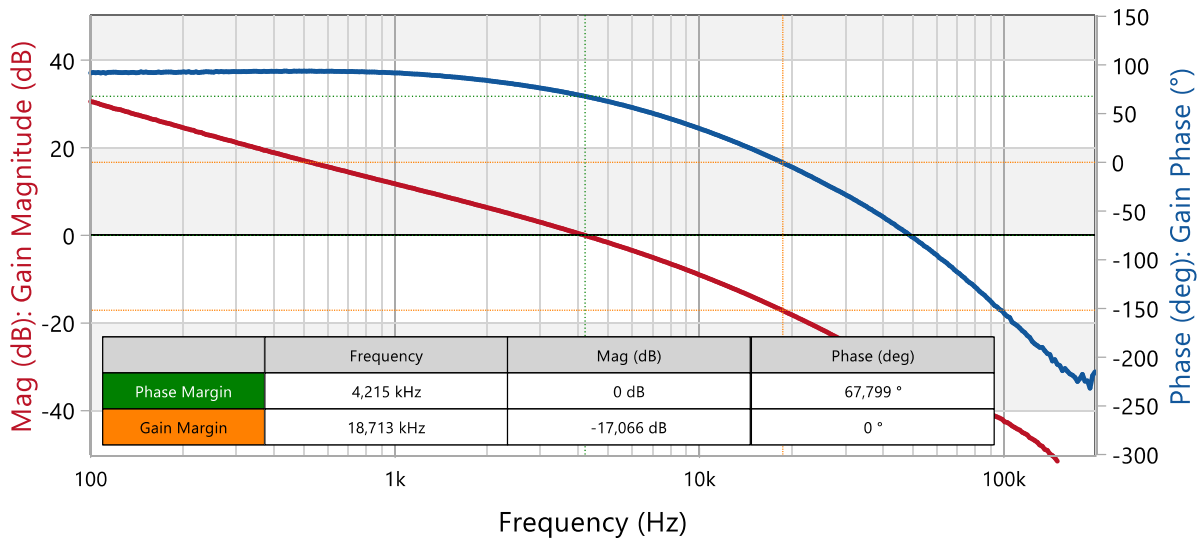
Figure 42: Measured open-loop response for compensator design 1 (WL-OCPT with CTR=0.9) (Vin = 36 V, Iout = 2.5 A) (Bode100™)

	Frequency	Mag (dB)	Phase (deg)
Phase Margin	13,101 kHz	0 dB	48,877 °
Gain Margin	30,838 kHz	-7,597 dB	0 °
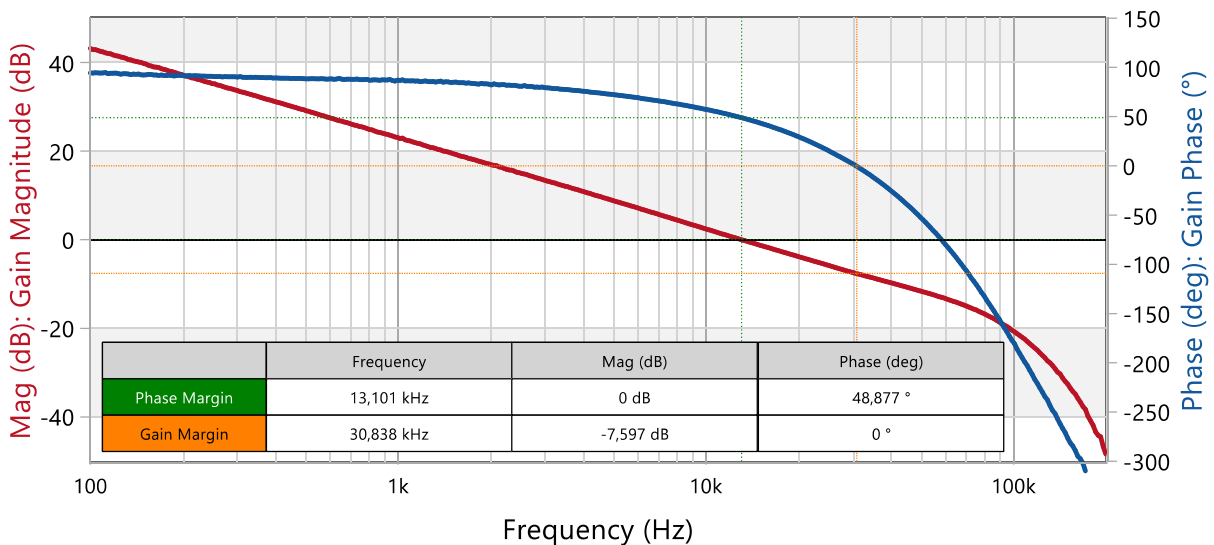
Figure 43: Measured open-loop response for compensator design 2 (WL-OCPT with CTR=0.9) (Vin = 36 V, Iout = 2.5 A) (Bode100™)

10.6 Test setup

Figure 44 shows the test setup used for frequency response measurement (open-loop response). A Bode100™ device with a B-WIT™ injection transformer both from Omicron Lab were used. A resistor load (4.7 Ω) draws 2.55 A output current (full load). Note that electronic loads should be better avoided for this test.
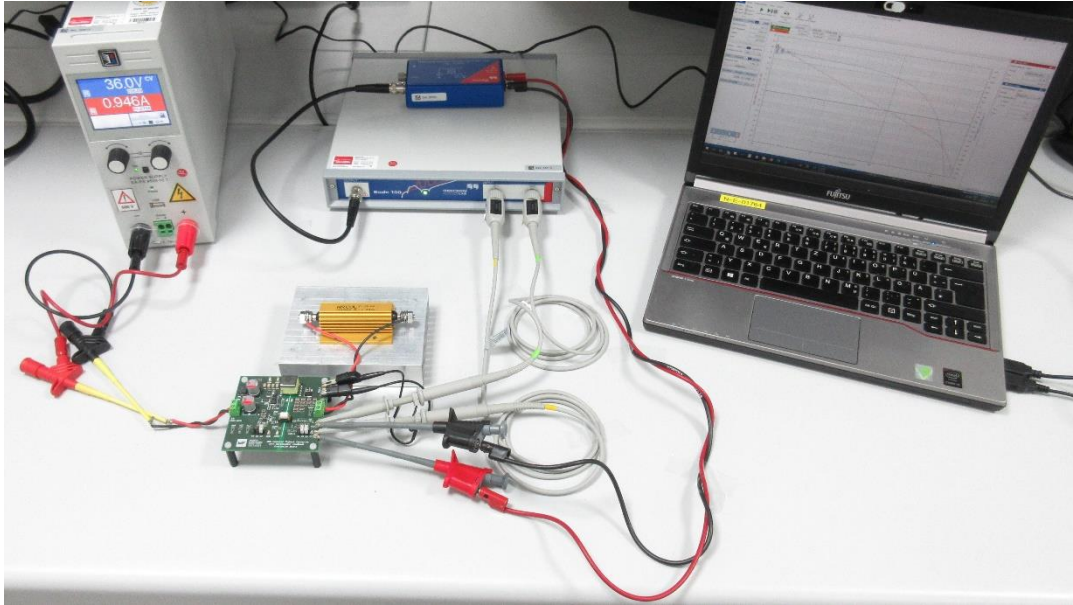
Figure 44: Test setup for transfer function / frequency response measurement

The test setup in Figure 45 was used to measure the load transients with a load current step of 2 A to 2.5 A. A 6-Ω resistor (2 x 3 Ω in series used in the setup) draws a constant output current of 2 A. A 25-Ω resistor is connected in parallel with the 6 Ω via a switched MOSFET with dynamic gate control. It draws the additional 0.5 A required for the load current step with the desired rise and fall dI/dt.
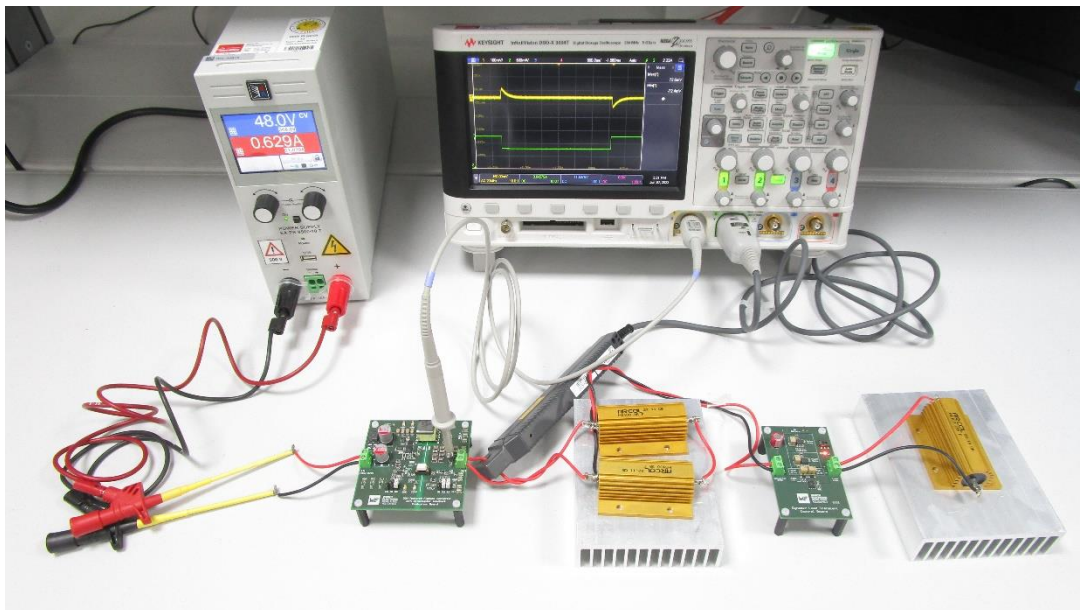
Figure 45: Test setup for load transient response measurement

011. SUMMARY AND CONCLUSION

Optocouplers are widely used to transmit the feedback signal across the isolation barrier in isolated power supplies. The optocoupler is therefore part of the compensator block and its parameters affect the compensator transfer function. A very popular compensator configuration uses a TL431 with an optocoupler, whose minimum current-transfer-ratio (CTR) value needs to be found for DC-bias design, and its full CTR range in order to analyze system performance. Variations in the CTR will shift the magnitude curve of the compensator transfer function up or down, leading to a different crossover frequency and in turn, a different phase margin of the open-loop transfer function. Another important consideration is the parasitic collector-emitter capacitance of the optocoupler phototransistor, which limits the optocoupler bandwidth. This parasitic capacitance is typically used to set the compensator pole for systems with low crossover frequency like offline AC-DC converters.

For higher crossover frequencies, like in the example shown in this document, the limitation of the optocoupler pole can be eliminated by introducing an additional zero and pole in the compensator. In any case, the optocoupler CTR and pole frequency play a key role in the control loop and their value and tolerance variations need to be considered in the design. Example procedures to find the CTR range as well as the optocoupler pole frequency have been provided, and their impact in the control loop has been shown. In addition to highlighting the optocoupler role in the system, the compensator design covered in this document illustrated a step-by-step example procedure to stabilize a current-mode Flyback converter operating in CCM.

A Appendix

A.1 Measuring WL-OCPT Optocoupler CTR

The current transfer ratio of the optocoupler can be measured in different ways and with different measurement equipment. In the example setup of figure 46, the voltage V_{dd} and the collector or emitter resistance value 'R' are both set as in the design (in this case: R = R_c = 5 kΩ, V_{dd} = 5 V). The same resistance value is selected on the LED side, and a signal generator is used to output a low-amplitude sinusoidal waveform with a DC offset adjusted to provide the required LED bias current to set V_{ce} to the target value (in this case V_{ce} = 2.7 V for full load, which gives V_2 = 2.3 V). With an oscilloscope, the voltages V1 and V2 are probed, and the CTR directly found by the ratio of the average values for DC, and the peak-to-peak values for AC, as below:

$$\text{DC CTR} = \frac{V_2}{V_1} \qquad\qquad \text{AC CTR} = \frac{\Delta v_2}{\Delta v_2} \tag{46}$$
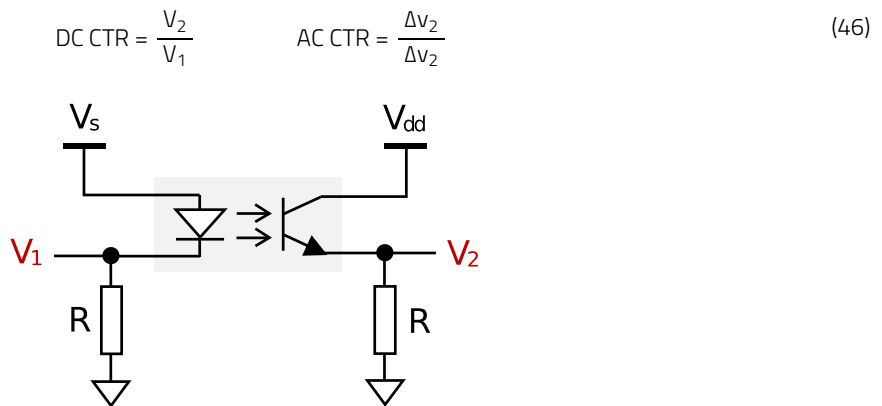
Figure 46: Example setup for measuring static and dynamic CTR values of WL-OCPT optocoupler

A.2 Measuring WL-OCPT Optocoupler Pole Frequency

The optocoupler pole frequency can also be measured with different techniques. Figure 47 shows an example measurement setup using a vector network analyzer (VNA) (e.g. Bode100™) with an injection transformer (e.g. B-WIT 100™). The setup considerations are like for the CTR measurement above, with the DC source V_{in} adjusted to provide the LED bias current required to set the target V_{ce} voltage. Note that voltages V1 and V2 should be checked with an oscilloscope at low frequency (at least a decade lower than the pole frequency) to ensure the sinusoidal waveforms are not clipped or distorted. If so, the amplitude of the injected AC voltage or the resistance R_s (normally between 10 and 100 Ω) will need to be reduced. A typical measurement result is shown in previous Figure 24.
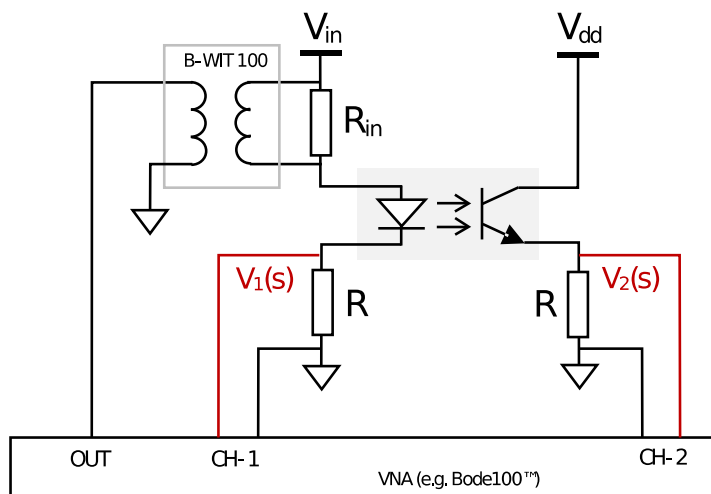
Figure 47: Example setup for measuring pole frequency of WL-OCPT optocoupler with a Vector Network Analyzer (VNA)

A.3 References

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